# VHDL Implementation of Channel Control Module for BiNoC Router

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***Abstract*— Novel BiNoC router architecture supporting the self configuring bidirectional channel mechanism is presented. The BiNoC allows each communication channel to be dynamically self configured to transmit flits in either direction in order to better utilize on-chip hardware resources. To facilitate this bidirectional traffic, we used a novel inter-router traffic control module known as Channel Control Module to allow neighboring routers to coordinate the specific directions of the pair of channels between them for each data packet. The flow direction at each channel is controlled by a channel direction control (CDC) algorithm. Implemented with a pair of finite state machines, this CDC algorithm is shown to be high performance, free of deadlock, and free of starvation. It is shown that the associated hardware overhead is negligible. This paper presents a VHDL based cycle accurate register transfer level model of inter-router traffic control module known as Channel Control Module for BiNoC architectures. The paper discusses in detail the architecture and characterization of the various inter-router traffic control mechanism in BiNoC router.**

***Keywords*-Interconnection networks, networks-on-chip, on-chip communication, reconfigurable architectures bidirectional channel.**

## I. INTRODUCTION

The Network On Chip is the emerging technique in the field of Very Large Scale Integrated Circuits (VLSI). Several multi-core integrated circuit designs such as 64 core SoC and 80-core NoC architecture [1][2] have been proposed recently. NoC uses a distributed control mechanism, resulting in a scalable interconnection network. Apart from throughput, NoC platform is scalable and has the potential to keep up with the pace of technology advances [3].

A NoC advocates a network communication design style: A general purpose communication backbone will first be deployed. Then application specific client logic (processors) can be mapped onto pre-allocated empty slots to form a complete system [4, 5]. NoC has the better improvement over the System On chip busses and also over the cross bar switches. Since the use of emerging NoC architecture in VLSI it reduces the size of the architecture due to the reduced amount of buses and transmission lines. This also reduces the power consumption while compared to the SoC ie; the requirement of source power in the SoC is high and it can be reduced by the NoC architecture.

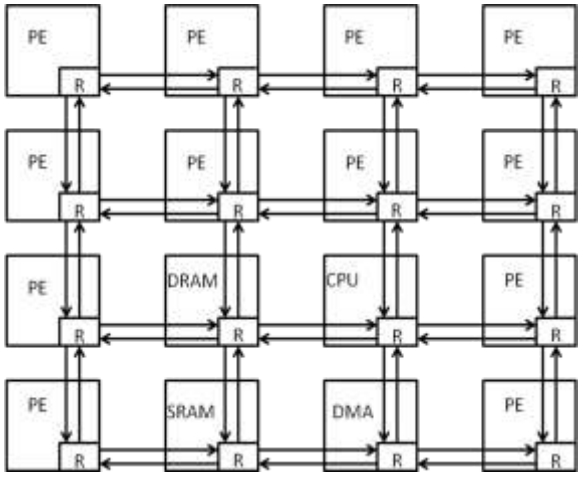



Fig 1.Typical NoC architecture in mesh topology

This NoC is used to communicate two or more Ip core in system On Chip (SoC).The NoC architecture can operate simultaneously on different data packets hence by using this NoC architecture the high level of parallelism is achieved.

A typical NoC consists of computational processing elements (PEs), network interfaces (NIs), and routers. The NI is used to packetize data before using the router backbone to traverse the NoC. Each PE is attached to an NI which connects the PE to a local router. When a packet was sent from a source PE to a destination PE, the packet is forwarded hop by hop on the network via the decision made by each router.

In this paper we concentrate on a novel part of the architecture-level adaptation namely the runtime bidirectional configuration control by channel control module. Bidirectional communication in the NoC typically employs fullduplex communication using two simplex links [6], [7]. We observed that there may be several scenarios as mention below where we may

require bidirectional configuration control to get improve channel bandwidth capacity.

a. Assuming all the transactions of flits are flowing in a single direction, there might be situations in inter-task connections where a certain link requires an increase in link capacity

b. Bandwidth requirements of transmission increases according to user requirement changes (e.g. the MPEG processing element (P.E.) wants to switch video resolution to a higher resolution). If in such a scenario current channel capacity of one half of the duplex channel cannot meet the requirement then the other half can be reversed to add more available bandwidth (doubled the channel capacity in our bidirectional router)

c. When a faulty situation occurs in a simplex channel, the transmission of flits via this channel will not possible. In such a scenario, if another simplex channel has the ability to reverse its direction while free, it could transmit flits. Therefore, it increases the resource utilization and improves reliability factors through channel control module.

To the best of our knowledge, there has been very little work which we are reviewing on bidirectional configuration control module for BiNoC architectures. In BiNoC router the ports are reconfigurable. The reconfigurations of ports are done by using the local information channel.

The rest of this paper is organized as follows. In Section II, we will discuss some of the background materials for on chip bidirectional interconnection and prior related research. In section III, Motivation. Further section IV, Baseline of bidirectional network on-chip (BiNoC) architecture. In section V, bidirectional CDC. Finally, in Section VI, experiment results shows final router RTL along with test bench waveform of HP and LP FSM which constitute channel control module. In last section, brief statements conclude this paper.

## II. RELATED WORK

Using NoC architecture the power consumption can be reduced. The power consumption can be reduced both in input as well as output ports. The router usually has five input output ports. Any port can send a data also the same port can receive the same data; the power consumption rate varies with respect to injection rate at the processor. The physical link in the router also has power consumption when the packet is delivered.

V. Soteriou et. al [8] illustrates Network aware of power consumption which responds to the bursts and dips in traffic by turning channels on and off at runtime.

As we described above the router can connect to either point to point link or from multipoint to multipoint link [9] investigates bidirectional and multi drop transmission line interconnect for on chip high speed network.

In an on-chip 2-D mesh with nearest neighbor connections there will always be two links in close proximity to each other, delivering packets in opposite directions [10]. The reconfiguration can be done rapidly in response to changing traffic demands.

A configurable on-chip communication 2X-Links to provide bidirectional transmission using tri-state logic presented. The directional decision process in [11] is centralized and configuration of each link in advance according to real time flit traffic.

A. Louri et. al [12] illustrates the impact of repeater insertion on inter-router links with adaptive control and eliminating some of the buffers in the router. Their approach saves appreciable amount of power and area without significant degradation in the throughput and latency.

## III. MOTIVATION

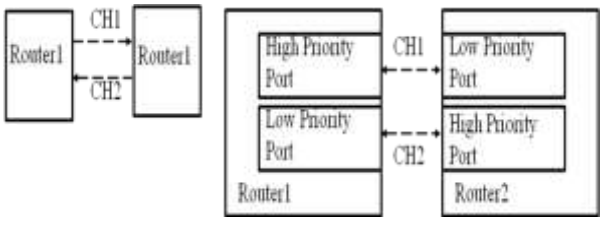



Fig.2 Channel direction in Typical NoC and propose BiNoC

In inter-routers communication scheme there are two simplex links i.e. one from Router 1 to Router 2 and another from Router 2 to Router 1. Both of these uni-directional links together form the full-duplex links. In BiNoC architecture, to get improve channel bandwidth, each channel have connection with high priority port on one side and low priority port on other side so as to avoid starvation and deadlock. Data transmission possible with channel direction in inter-router scheme as shown in fig.2

Our contribution -

We present VHDL implementation of a runtime bidirectional configuration control known as channel control module at the architecture-level to complement our existing adaptive on-chip communication infrastructure. The channel control module can adapt the channel capacity by changing the direction at runtime on demand, thereby increasing the resource utilization while considering the reliability issues. The building blocks of channel control module consist of a pair of finite state machines to allow neighboring routers to coordinate the specific directions of the pair of channels between them for each data packet.

## IV. BIDIRECTIONAL CHANNEL ROUTER ARCHITECTURE

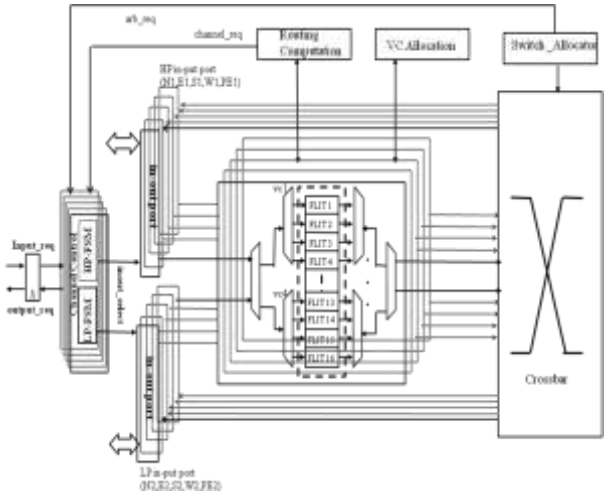



Fig.3 Modified Virtual channel router architecture for our BiNoC router with four state pipelines.

The heart of an on-chip network is the router, which undertakes crucial task of coordinating the data flow. Router is the most important component for the design of communication back-bone of a NoC system. In a packet switched network, the functionality of the router is to forward an incoming packet to the destination resource if it is directly connected to it, or to forward the packet to another router connected to it. In the NoC architecture there are two routers the conventional router and the bidirectional router. In this conventional router the data can be send in only one direction whereas in bidirectional router the data can be send and receive simultaneously. The Bidirectional Network on Chip (Bi-NoC) architecture is more efficient than the conventional architecture because in conventional architecture the unidirectional flow is used where as in Bi-NoC the two way data flow can be performed [13]. The XY routing algorithm is used to perform the architecture. The Bi-NoC architecture allows each channel to transmit in all direction and increases the bandwidth, reduces the access latency, and reduces power consumption.

### *A. Reconfigurable Input/Output Ports*

The ports in the bidirectional are reconfigurable. This is done by using the local information.

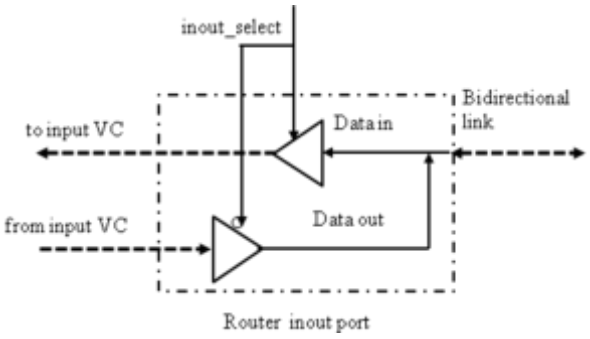



Fig.4 Schematic of Reconfigurable Input/Output Ports implemented in BiNoC architecture.

As shown in Fig. 4, the input and output port used in bidirectional NoC architecture is based on the priority. In this one port is designed with the higher priority and the other port is designed with the lower priority. A channel control protocol is used to determine its own transmission direction from a router to another router. By this bidirectional ports doubling of channel bandwidth is possible.

## V. On Chip Channel Direction Control Module

The flow direction at each channel is controlled by a channel direction control (CDC) algorithm. Two major functions performed by the channel control algorithm.

1. Dynamically configure the channel direction between neighboring routers.

The control algorithm is implemented with two finite state machines. The current status of channel direction decides whether the channel request for corresponding channel is blocked or not.

2. To process the channel allocation by sending arbiter request to the switch allocator.

The channel direction control algorithm replaces all the unidirectional channels in a typical NoC with bidirectional channels. The HP and LP ports of each router use two FSMs, a HP FSM and a LP FSM are connected to bidirectional channel. Pair of signals input−req and output−req is used to exchange information between two FSMs.

### *A. Bidirectional Channel Direction Control*

The finite state machine diagrams for a High priority and a Low Priority Channel Direction Control algorithm are shown in Fig.5 (a) and (b), respectively. Each FSM has three states: free, wait, and idle.

a) Free State: the channel is ready for data to send (output) the adjacent router.
b) Idle state: the channel is available to receive (input) data from the adjacent router.
c) Wait state: it is an intermediate state ready to transition from idle state with input channel to free state with output channel.

The operations of the HP FSM and the LP FSM are discussed below.

*a. HP FSM Operations:*

The operation of HP FSM explain with different Case for each state

Case I- when current router has data packets, HP FSM always initiated with free state. As long as input_req=0 or channel_req=1,HP FSM remain at free state that's means channel direction remain outbound even when there is no flits to send or there is no request to transmit from neighboring router .the output signal of free state is output_req=channel_req.

Case II- when there is flits to be sent from neighboring router, HP FSM will leave the free state and enter into an idle state. As channel _req=0 HP FSM will remain in idle state and channel direction is outbound. Output signal is output_req=1.

Case III-when channel_req=1, HP FSM will get into a wait state to acquire the channel control to send flits. Output signal at wait state is output_req=1 and counter will increase during every clock. When count equal 2, HP FSM regain to the free state and starts transmitting flits and at the same time counter will reset to zero.

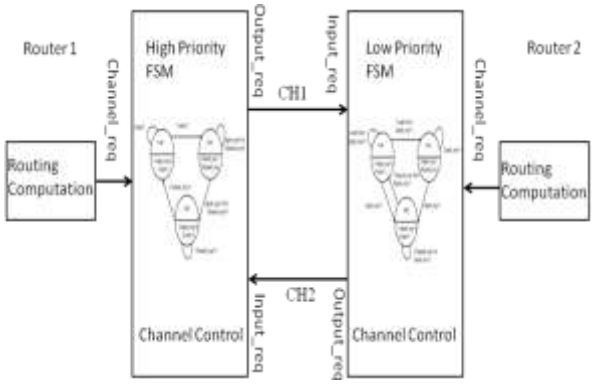



Fig. 5 (a) FSM for HP port and (b) FSM for LP port for bidirectional channels between two neighbouring routers .

b. *LP FSM Operations:*

The operation of LP FSM explain with different Case for each state

Case I- when channel_req=0 and input_req=1, the LP FSM always initiated with idle state and output signal is output_req=0. When other router want to send flits channel with input_req=0 and current router channel with channel_req=1

Case II- Due to low priority end of flits transmission, for four clock cycles LP FSM remain in the wait state. Within four clock cycles, if HP FSM want to send flits with input_req=1, LP FSM will return to an idle state. If count equal to 4 and input_req=0, the LP FSM will enter into a free state and start sending flits.

Case III- when input_req=0, the LP FSM enter into free state as long as HP FSM does not have any flits to transmit. As soon as input_req=1, the LP FSM stop transmitting flits immediately and return to and idle state.

## VI. Experimental Results

### *A. Performance Evaluation*

In this section, we present simulation-based performance evaluation of our architecture, BiNoC router with Self-Reconfigurable Channel using Channel Control Module. We describe our experimental methodology, and detail the procedure followed in the evaluation of these architectures.

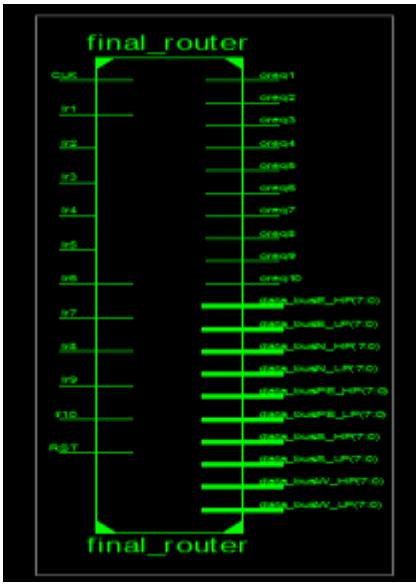
### *B. Simulation setup*

In this section the synthesis results will be presented. The proposed BiNoC routers with Self-Reconfigurable Channel using Channel Control Module were implemented in structural Register- Transfer Level (RTL) VHDL. A Router with parametrable flit size and 4 flits buffer depth and Ten ports have been modeled with VHDL language on RTL level. They were simulated and synthesized respectively by using the ISE 13.1 tool.

### *C. Self-Reconfigurable Channel using Channel Direction Protocol Validation*

The Channel Control Module was described in VHDL and validated by functional simulation. Fig.6 shows functional simulation result of Self-Reconfigurable Channel using Channel Control Module in BiNoC router. This simulation is performed on Active-HDL software.

*a. Final Router RTL*



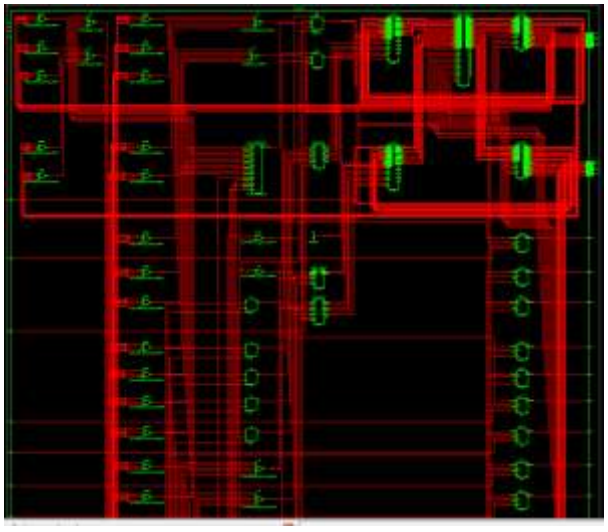
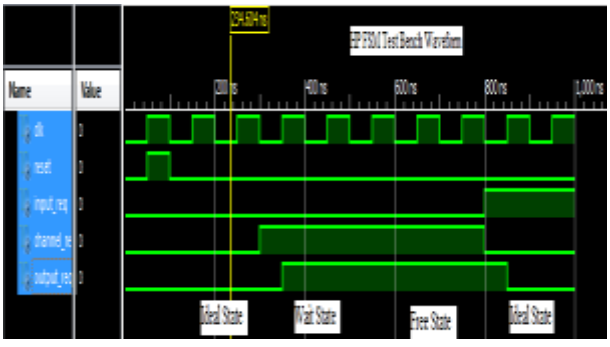


Fig. 6 Final BiNoC Router RTL

*b. FSM Test Bench Waveform*



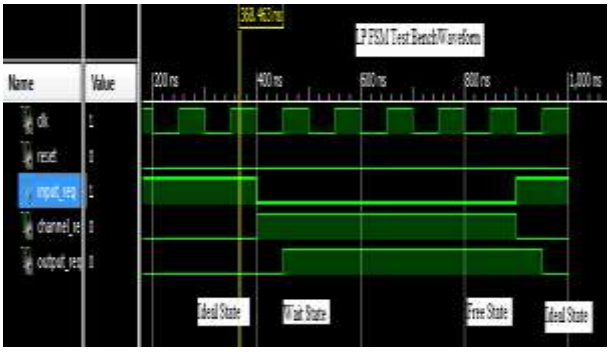




Fig. 7 FSM Test Bench Waveform

*D. Area Measurement*

BiNoC router architectures in terms of logic gate count and percentage calculated by synopsys design compiler [40].

Area and Power breakdown of BiNoC_4VC

Table I
Area breakdown of *BiNoC_4VC* [14]

| Component buff. Depth | BiNoC_4VC(16) 4 flits x 4 | |
|---|---|---|
| | Area (gate count) | Power (mW) |
| **Input buf. + buf. ctrl** | 18,722 | 16.90 |
| **Routing computation** | 669 | 0.48 |
| **VC allocation** | 12,295 | 5.76 |
| **Switch allocation** | 2,245 | 1.75 |
| **Switch traversal** | 4,402 | 2.35 |
| **Bidir. ch. ctrl** | 1,628 | 0.68 |
| **Total** | 39,960 | 27.94 |

## VII. Conclusion

In this paper, we represented a novel NoC backbone architecture BiNoC which features dynamically self reconfigurable bidirectional channels. A Channel Control Module that supports real-time traffic-direction arbitration in the bidirectional channels while avoiding deadlock and starvation. The architecture prototyped on a Spartan 3A FPGA based Self-Reconfigurable Channel using Channel Control Module in BiNoC system. We have implemented an accurate hardware model for Self-Reconfigurable Channel using Channel Direction control module with VHDL.

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