Design of One Bit Arithmetic Logic Unit (ALU) in QCA

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***Abstract* –Quantum cellular automata (QCA) is a new technology in nanometre scale as one of the alternative to nano technology. QCA technology has large potential in terms of high space density and power dissipation with the development of the faster computer with low power consumption. We describe the design and layout of a simple 1-bit ALU based on quantum-dot cellular automata (QCA) using the QCADesigner design tool. The ALU design is based on combinational circuits which reduces the required hard-ware complexity and allows for reasonable simulation times. Our aim is to provide evidence that QCA has potential applications in future computers provided that the underlying technology is made feasible. We have design certain combinational circuit by using Majority gate, AND, OR, NOT, X-OR in QCA. In the combinational circuits, we have design Logical Extender, Arithmetic Extender and Full Adder are major blocks of one bit ALU.**

***Keywords* - ALU, Nano-technology, QCA.**

I. INTRODUCTION

Quantum Dot cellular automata (QCA) is an attractive emerging technology that takes advantage of quantum effects, which become increasingly apparent at the scale of a few nanometers. Previous work has shown that QCA has several novel features not available with conventional FET-based circuits [1]. Although the design cost function is different from FET-based technologies [2], a significant effort has already been started into exploring alternative arithmetic architectures that are portable to QCA, such as systolic arrays and bit-serial circuits. Recently, several successful studies into computer arithmetic and memory structures have provided further motivation for research into the realization of QCA technology [2-8].

The QCA cell [9] consists of a system of four quantum dots charged with only two free electrons. Electrostatic repulsion between these electrons force them to occupy only the diagonal sites creating a so called "polarization" used to encode binary information, as seen in Figure 1. Interactions between neighboring cells allow for the layout of functional circuits, where the objective is to layout the cells in such a way that the ground state polarization of the output cells represents the correct output of a function to a given set of input vectors.

To date, proof of concept QCA cells have been experimentally verified using a device which exploits the Coulomb blockade phenomenon [10], although the originally proposed cell is still beyond present fabrication capabilities. As a result, investigators are currently looking at creating QCA cells using single molecules [11].

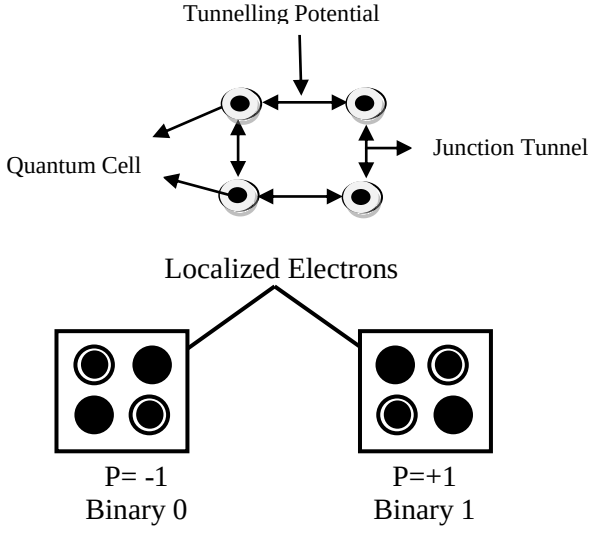
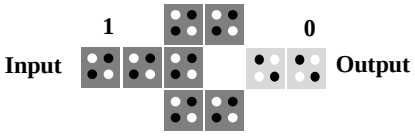


Fig 1: QCA Cell

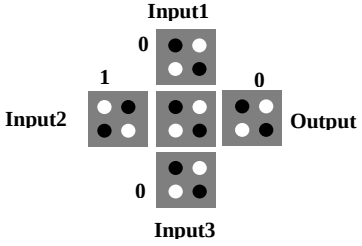
At first, it may appear premature to begin in depth investigations into the design of large circuits such as the one proposed here prior to the realization of a final technology. However, due to the capabilities of today computers, the cost of such investigations is relatively low when compared to experimental studies. Such investigations provide a feedback mechanism in the development loop that can fairly rapidly include or

exclude new device implementation concepts based on their potential application in these larger circuits. Using simulations we have, for example, identified a fundamental requirement for multilayer capability in complex circuits, previously believe unnecessary [12].

The physical interactions between cells may be used to realize elementary Boolean logic functions. The basic logic gates in QCA are the Majority logic function and the Inverter which are illustrated in Fig. 2. The Majority logic function can be realized by only 5 QCA cells. The logic AND function can be implemented from a Majority logic function by setting one input permanently to 0 and the logic OR function can be Implemented from a Majority logic function by setting one input permanently to 1.



(a) QCA Inverter



(b) QCA Majority Voter

Fig 2: QCA Logic Gates

II. QCA Clocking and Device Level Latching

Unlike the transistor, a basic QCA cell has no inherent directionality for information flow, and a circuit made of un-clocked cells would propagate information in uncontrollable directions. In order to control the flow of information in a QCA circuit, four clock signals, each shifted in phase by 90*o*, as shown in Figure 3, are used [13,14]. These clock signals are expected to be generated by a supporting technology such as a CMOS circuit which is used to control the tunneling ability of electrons within the cell.

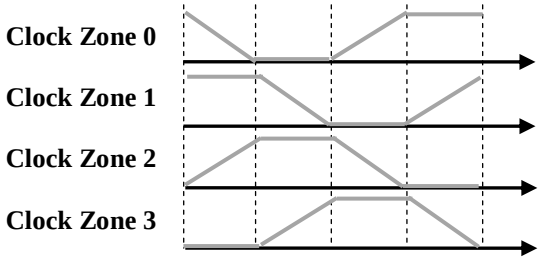


Fig 3: QCA Clocking Zones

The clock signals act to pump information in controlled directions in the circuit as a result of the successive latching and unlatching in cells connected to different clock phases. For example, a wire, which is clocked from left to right with increasing clocking zones, will carry information in the same direction; i.e., from left to right. This acts to pipeline QCA circuits at a device level. QCA wires allow more than one bit of information to be propagated along the same wire at any one time. When the clock drops it latches the cells into one of two possible polarizations based on the influence of all its neighboring cells. When the clock signal is high, the cells are relaxed, and have no polarization. The minimum size of the clocking zone is determined by the minimum feature size of the technology used to support clocking. Large clocking zones can be problematic because signals traveling down long QCA wires have increased probability of error from outside influences. These include thermal effects, which can potentially flip the state of a cell. Small clocking zones allow the designer the ability to create more complicated and dense circuits. They also decrease the probability of error in the circuit. However, smaller clocking zones are generally more difficult to fabricate.

III. QCA Information Flow

Switching is driven by perturbations introduced by outside influences, such as neighboring cells, which cause the cell to switch from one polarization to another as illustrated in Fig. 4. This involves the transfer of electrons between the sites of the cell, which is made possible due to quantum mechanical tunneling. Quantum tunneling enables particles to be transmitted through potential barriers without having the required energy to overcome the barrier. The design of QCA circuits involves finding a layout of cells, where the ground state of the layout for a particular set of boundary conditions provided by the inputs is the solution to the designed logical function. By providing a suitable environment, the cell will relax to the ground state. Changes in the boundary conditions (input values) cause the system to relax to a new ground state, and a new output. Unfortunately, computing with the ground state implies that the system is sensitive to temperature effects. In order for the system to be thermodynamically robust, the kink energy, E_{kink}, and other relevant energies must be larger than the thermal ambient energy K_BT.

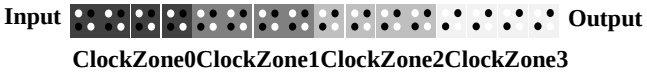


Fig 4: QCA Wire

IV. Architecture of ALU

The Arithmetic Logic Unit (ALU) performs the basic arithmetic and logical operation and consists of arithmetic extender, logical extender and one bit full adder as shown in figure 5.

Three control signals determine the operation of the ALU. M is the mode control variable used to select between arithmetic and logical operations. S1 and S0 are used in combination with M to select between the eight arithmetic and logical operation the ALU supports.

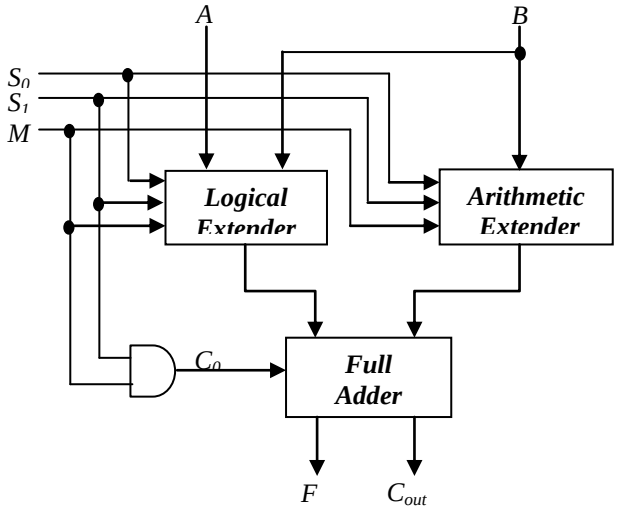


Fig 5: Architecture of ALU

A. Arithmetic Extender

The Arithmetic extender modifies the second operand and passes it to the Full adder to the arithmetic.

TABLE I
FUNCTION TABLE OF ARITHMETIC EXTENDER

M	S_1	S_0	Function name	Function	X	Y	C_0
1	0	0	Decrement	A-1	A	all 1's	0
1	0	1	Add	A+1	A	B	0
1	1	0	Subtract	A+B'+1	A	B'	1
1	1	1	Increment	A+1	A	all 0's	1

TABLE II
TRUTH TABLE OF ARITHMETIC EXTENDER

M	S_1	S_0	B	Y
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	1	0	0
1	1	1	0	0
1	1	1	1	0

According to truth table we write Boolean equation of arithmetic extender shown in equation (1) and design logic circuit of arithmetic extender shown in fig. 6.

$$Y = M\bar{S_1}B + M\bar{S_0}\bar{B} \quad \ldots (1)$$

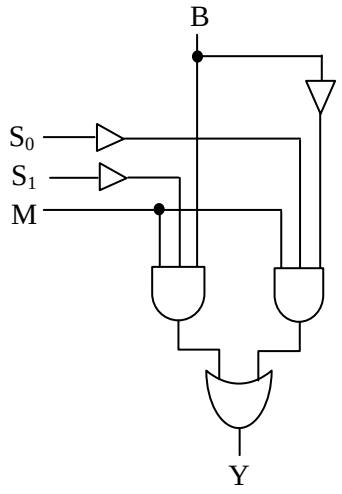


Fig 6: Logic Circuit of Arithmetic Extender

B. Logical Extender

The logic operations are performed in the logic extender. The FAs are used simply as connection for the outputs.

TABLE IIII
FUNCTION TABLE OF LOGICAL EXTENDER

M	S_1	S_0	Function Name	Function	X	Y	C_0
0	0	0	Complement	A'	A'	0	0
0	0	1	AND	A and B	A&B	0	0
0	1	0	Identity	A	A	0	0
0	1	1	OR	A or B	A|B	0	0

TABLE IIIV
FUNCTION TABLE OF LOGICAL EXTENDER

M	S_1	S_0	X
0	0	0	A'
0	0	1	A & B
0	1	0	A
0	1	1	A | B
1	X	X	A

According to truth table we write Boolean equation of logical extender shown in equation (2) and design logic circuit of logical extender shown in fig. 7.

$$X = \bar{M}\bar{S_1}\bar{S_0}\bar{A} + \bar{M}S_1S_0B + S_0AB + S_1A + MA \quad \ldots (2)$$

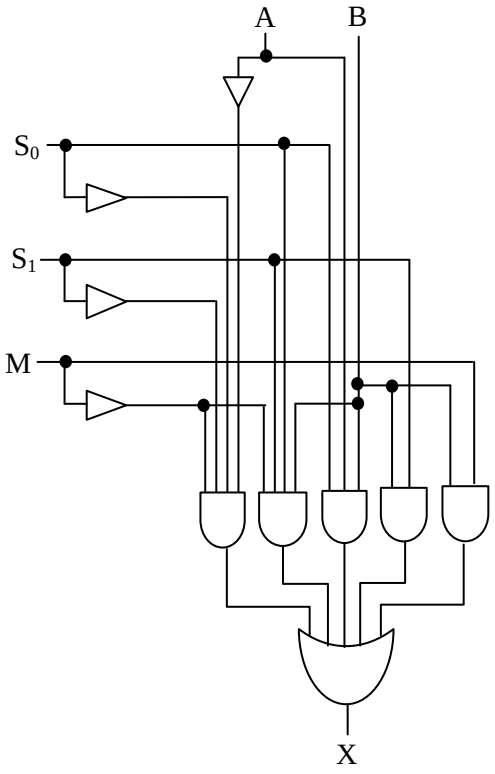


Fig 7: Logic Circuit of Logical Extender

C. Full Adder

Full adder performs the addition of three bits. In full adder, we have given three inputs X, Y and C_0, where C_0 is carry in signals shown in equation (3).

$$C_0 = MS_1 \quad \ldots (3)$$

TABLE V
TRUTH TABLE OF FULL ADDER

X	Y	C_0	F	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The Boolean equations for Full adder are shown in equations (4) & (5) and logic circuit of full adder as shown in figure 8.

$$F = X \oplus Y \oplus C_0 \quad \ldots (4)$$
$$C_{out} = MV(X, Y, C_0) \quad \ldots (5)$$

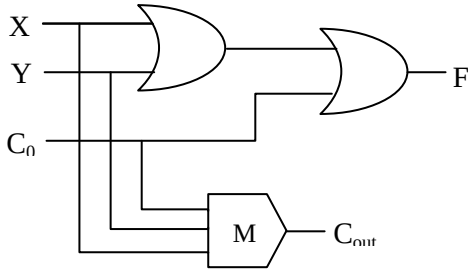


Fig 8: Logic Circuit of Full adder

V. IMPLEMENTATION OF ALU IN QCA

Implementation of one bit ALU in QCA is verified using QCA Designer tool. The proposed design is shown in Figure 9.

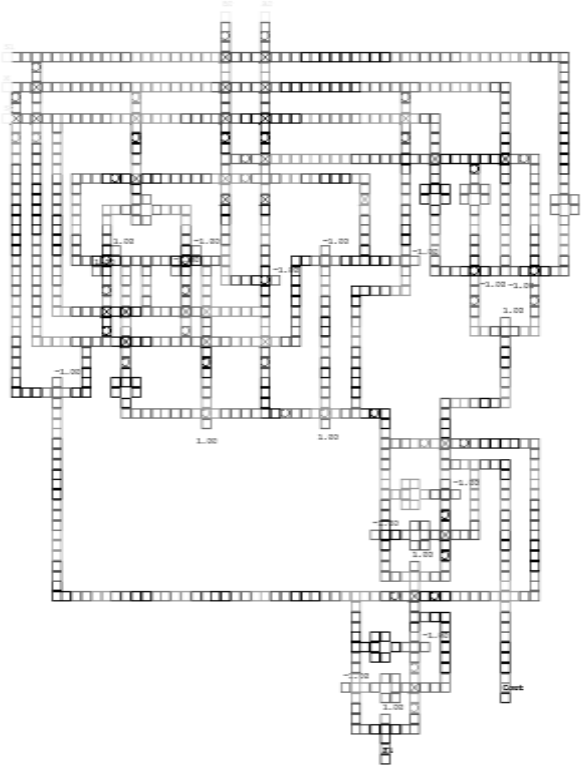


Fig 9: QCA layout of one bit ALU

VI. SIMULATION RESULTS AND DISCUSSION

All the designs were verified using QCADesigner tool ver. 2.0.3. In the bi-stable approximation, we used the following parameters: cell size=18 nm, number of samples=12800, convergence tolerance=0.001000, radius of effect=65.00 nm, relative permittivity=12.900000, clock high=9.800000e-022, clock low=3.800000e-023, clock amplitude factor=2.000000, layer separation=11.500000, maximum iteration per sample=100. All of these parameters which used are default parameters in

QCADesigner tool. In our QCA layouts, we have the goal of workable designs with compact layout. The simulation Results of one bit ALU is shown in figure 10. According to simulation results, as we seen the highlighted area is the output of ALU and the QCA circuit of ALU has delay of 9 clocks. This result shows the outputs are same as truth table of ALU.

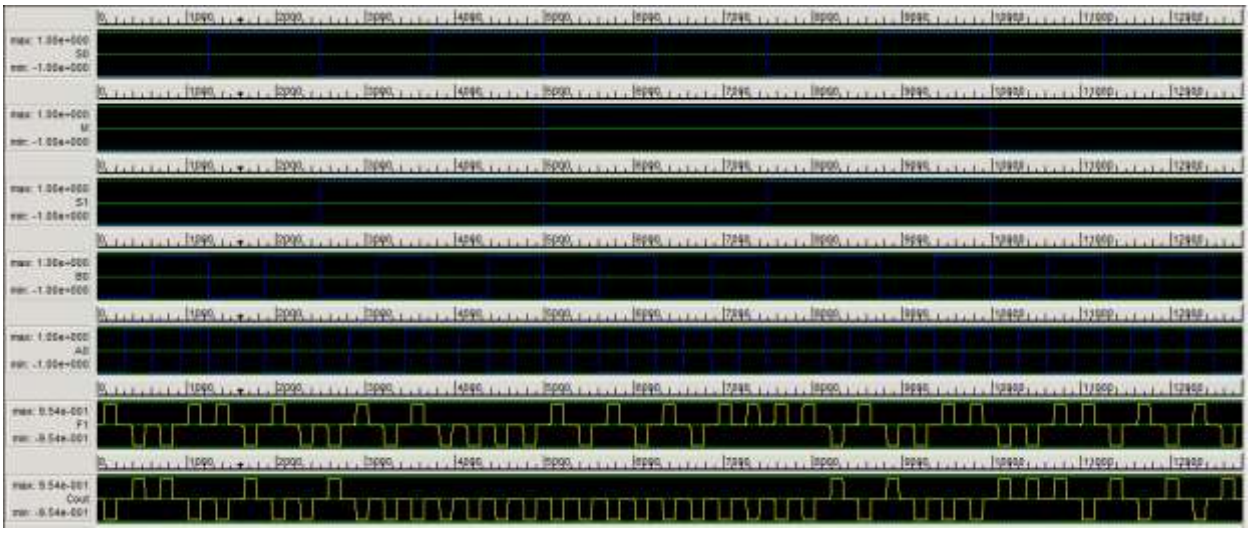


Fig 10: Simulation results of One bit ALU

VII. Conclusion and Future Work

This paper proposes one bit ALU (Arithmetic Logic Unit) in QCA which uses arithmetic and Logical Extender and Full adder. The proposed work shows that the Functions of ALU design in QCA is same as traditional ALU designed in CMOS technology. By using QCA we have reduces complexity, size, power consumption, delay & cost and Improve the performance of ALU is much beneficial.

In future, we will design 2-bit, 4-bit & 8-bit ALU in QCA. We will also design 1-bit ALU (Arithmetic Logic Unit) using Reversible logic gates in QCA.

Acknowledgement

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