A Gain Flattened LNA by using Drain- Fully-Differential Active Inductive Gain-peaking Technique

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***Abstract*— A flat gain and low-noise amplifier for digital TV tuners is presented in this paper. The low noise characteristic of the LNA is achieved by the noise cancelling technique and the gain flatness is enhanced by the drain-inductive gain-peaking technique by using an active inductor in CMOS technology in drain of noise cancelling cascode amplifier. In this design we used 0.18µm RFCOMS transistor and Advanced Design system (ADS) for Design and simulation circuits. The LNA gain can be tuned from 17.375 dB to 17.489 dB. The gain variation of the LNA is ±.114 dB from 50 to 900 MHz. The measured noise figure of the CMOS LNA is 2.088 dB.**

***Keywords*— LNA, Flatness,**

I. INTRODUCTION

The noise figure of the overall receiver in a telecommunication system depends on the first element following the antenna, the Low Noise Amplifier (LNA). The main function of the LNA is to provide high enough signal gain to overcome the noise of the subsequent stages while adding the minimum possible noise [1].

Television broadcasting was allocated a wide frequency spectrum below 900 MHz. The low noise amplifier is an essential component in a wideband receiver, and its characteristic is closely related to the receiver sensitivity and dynamic range. Gain flatness of the LNA is often overlooked in many RF applications because of narrow allocated bandwidth. However, it deserves more attention for wideband applications because gain flatness can not only facilitate roughly the same signal amplification across the whole spectrum in the downstream receiver path, but also relax the dynamic range requirement of the analog-to-digital converters (ADCs) in the wideband receivers [2].

As to the inductive peaking design, by using the gate and drain inductive peaking approach, the 3-dB bandwidth could be both improved; moreover, the drain-inductive peaking demonstrated the superior characteristics in the output eye patterns [6].

In this paper, the Drain-inductive gain-peaking technique is presented by using a differential active inductor [3] in CMOS technology in drain of noise cancelling cascode amplifier to have wideband flat gain.

By using this technique, The measured power gain of the LNA is 17.34 dB with 0.114 dB gain variation from 50 MHz to 900 MHz. Operated at 1.8 V. The measured noise figure of the CMOS LNA is 2.088 dB.

II. NOISE-CANCELLING TECHNIQUE

Since originally proposed to reduce the noise figure of the feedback amplifiers at low gigahertz frequency range [5], noise cancelling technique has become a popular technique for designing wideband LNAs.

Fig. 1 shows a block diagram of Wideband gain-flattened LNA architecture. Fig. 2 shows a simplified realization of the concept in Fig. 1. The channel thermal noise of the matching device M1, which is a dominant noise component in a submicron CMOS device, can be modelled as a noise current source In. A portion of this thermal noise current αIn flows out of M1 through R_f and R_S, where $0 < \alpha < 1$, and causes two correlated noise voltages at nodes X and Y, which are in phase and can be expressed:

$$V_{X,n} = \alpha I_n R_S \quad (1)$$
$$V_{Y,n} = \alpha I_n (R_S + R_f) \quad (2)$$

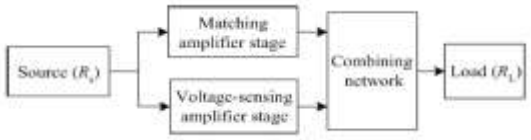

Fig1. Wideband gain-flattened LNA architecture.

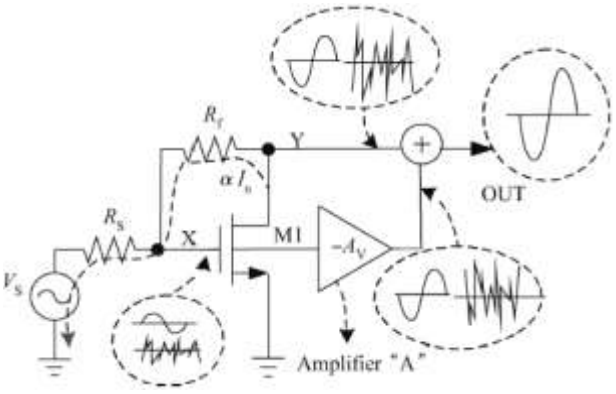

Fig2. Wide-band LNA exploiting noise-cancelling technique.

Meanwhile, because of the negative gain of the common source amplifier, the signal voltages at nodes X and Y are in opposite phases. This difference in noise and signal makes it possible to cancel the noise of the matching device M1 while adding the signal contributions constructively. It can be done by adding a negatively scaled replica of the voltage at node X to the voltage at node Y as illustrated in Fig. 2. The output noise voltage after noise cancelling operation can be derived as:

$$V_{OUT,n} = \alpha I_n (R_S + R_f) + \alpha I_n R_S \qquad (3)$$

Output noise cancelation, $V_{OUT,n} = 0$, is achieved when the gain $A_v$equals:

$$A_v = 1 + \frac{R_f}{R_S} \qquad (4)$$

Since the signal components at node X and Y have the opposite polarity, the signal gain is actually enhanced after noise cancelling operation. Assuming the input impedance of the amplifier matches the source impedance, the overall signal voltage gain can be shown as:

$$G_V = -2\frac{R_f}{R_S} \qquad (5)$$

III. Drain-Inductive Gain-Peaking Technique

In this paper, the Drain-inductive gain-peaking technique is presented by using a differential active inductor [3] in CMOS technology in drain of noise cancelling cascode amplifier to have wideband flat gain.

In this article a 0.18 µm CMOS differential active inductor with tuneable L is used for Drain-inductive gain-peaking technique [3].

A. Active Inductor

A novel CMOS active inductor is shown in Fig.3. The proposed circuit topology resembles the classical gyrator-C inductor architecture. with the n-channel common-gate transistor M_{n1} and pchannel common-source transistor M_{p2} implementing an active gyrator and the gate-source capacitance of M_{p2} (C_{gs2}) perfomning the integration. The circuit simulates a grounded inductor which appears in parallel with the gate-source capacitance of M_{n1} (C_{gs1}). The equivalent small-signal input impedance Z_{in} is the parallel combination of C_{gs1} ,$\frac{1}{g_{ds2}}$ [10].

$$L_{eq}(w) = \frac{C_{gs2}\ (1-w^2\frac{C_{gs2}}{gm_1 gm_2}C_{gd2})}{gm_1 gm_2(\left(1-w^2\frac{C_{gs2}}{gm_1 gm_2}C_{gd2}\right))^2+w^2\frac{(C_{gs2}gm_1+C_{gs1}gm_2)}{gm_1 gm_2}} \qquad (6)$$

$$R_s(w) = \frac{\frac{g_{ds1}}{gm_1 gm_2}+\frac{1}{gm_1}\left(1+\frac{\frac{gm_2}{C_{gs2}}}{\frac{gm_1}{C_{gs2}}}\right)(\frac{w}{\frac{gm_2}{C_{gs2}}})^2}{\left(1-w^2\frac{C_{gs2}}{gm_1 gm_2}C_{gd2}\right))^2+w^2\frac{(C_{gs2}gm_1+C_{gs1}gm_2)}{gm_1 gm_2}} \qquad (7)$$

The magnitude of g_{ds1} determines the lower-end of the bandwidth of the inductive characteristic.

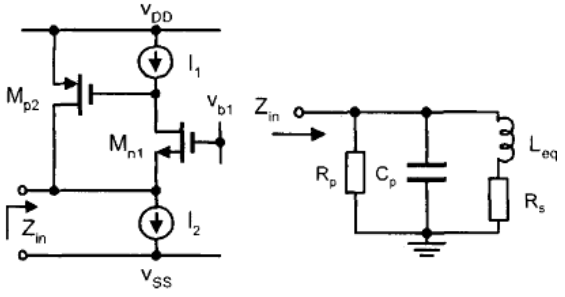

Fig3. A novel RF CMOS grounded active inductor and its small-signal equivalent circuit model.

Thus high-Q and wide operating bandwidth active inductors can be realized by reducing g_{ds1} .This can be achieved by applying either cascode or negative resistance cancellation techniques to the active inductor [7]-[8].

At high frequencies, close to the self-resonance, R_s rises and reducing g_{ds1} alone has insignificant effects to the high-frequency loss (i.e. the real part of Z_{in}) of the simulated inductor. It is easy to show that decreasing the magnitude of g_{ds2} reduces the high frequency loss of the active inductor more effectively [9]. Furthermore, this can be obtained by using either cascode or negative resistance cancellation techniques.

B. Fully-Differential Active Inductor

The advantage of the single-ended active inductor is low noise figure due to the circuit simplicity. However, in high-frequency circuits, balanced operation is usually preferable due to the benefits of increased dynamic range and noise rejection ability. A fully differential floating active inductor can be realized by using two identical single-ended active inductors as shown in Fig. 4. Both cascode and negative resistance cancellation techniques are employed to enhance the quality factor and operating bandwidth of the inductor. Cascode transistors M_{p3a}, M_{p3b} and cross-coupled transistors M_{p4a}, M_{p4b} reduce the output conductance of M_{p2a}, M_{p2b} (i.e. g_{ds2}) and M_{n1a}, M_{n1b} (i.e. g_{ds1}) respectively [10].

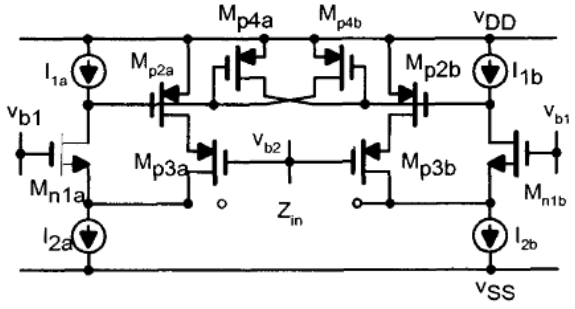

Fig4. High-Q fully-differential floating active inductor.

In Fig. 5, simulation result of inductance value of designed active inductor is shown.

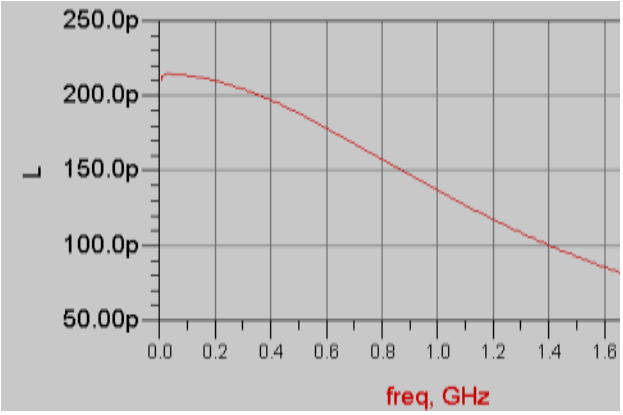

Fig5.Simulation result of inductance value of active inductor

IV. Circuit Design

The circuit schematic diagram of the gain-flattened CMOS LNA is shown in Fig. 6. The matching amplifier stage consists of M_{n1} and M_{p1}. Because of the shunt-feedback resistor (R_F) the amplifier gain is flattened .Moreover, by increasing R_F , noise figure and gain are improved but it corrupted input matching. The noise cancelling amplifier stage consists of the cascode amplifier M_3 and M_2. The matching stage is ac coupled to M_4 via the high-pass filter formed by R_1 and C_2.

The current bleeding technique [11] is used to provide additional bias current for the noise cancelling amplifier such that the noise cancelling amplifier can be tuned for performance without consuming too much power on the source follower. Since both the matching amplifier stage and noise cancelling stage have good gain flatness, excellent overall gain flatness and noise cancelling result are achieved.

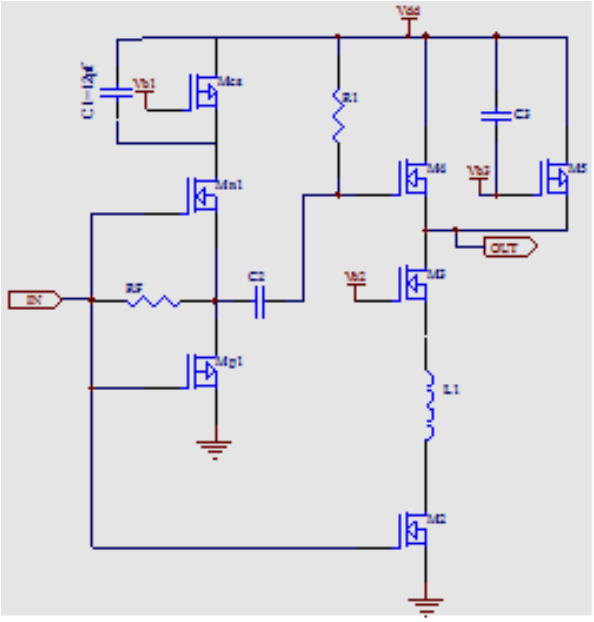

Fig6. Circuit diagram of the drain-inductive-peaking CMOS LNA.

V. Simulation Results

The wideband LNA with drain-inductive-peaking and noise-cancelling techniques is designed and simulated with ADS software in TSMC 0.18 _m RF CMOS technology.

Noise figure diagram is shown in Fig.7, according simulation result noise figure of circuit is below than 2.088 for frequency below than 1GHz .

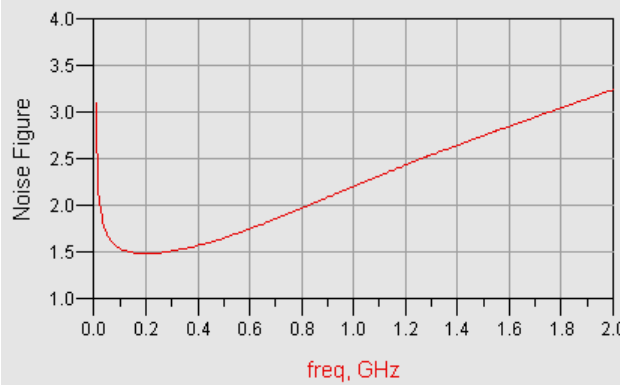

Fig7. Noise figure of simulated LNA.

Gain according frequency diagram is shown in Fig.8, according to simulation result gain is about 17.34dB and the flatness of gain is about ±0.114 dB for frequency below than 1GHz .

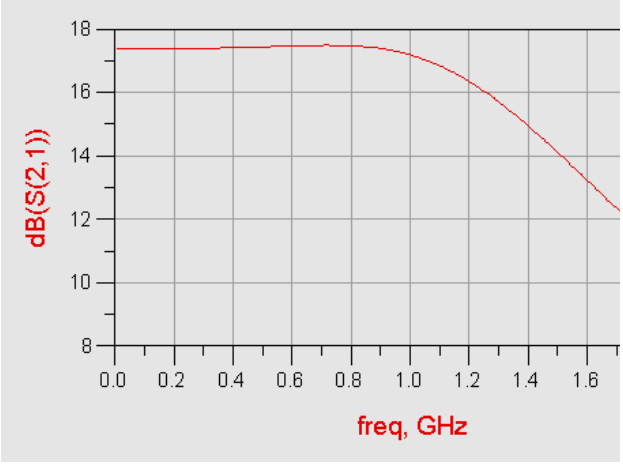

Fig 8.Gain of simulated LNA

Input and output matching according frequency diagram is shown in Fig.9, according to simulation result of circuit S_{11} is below than -10dB and S_{22} is below than -14dB for frequency below than 1GHz .

S_{12} According frequency diagram is shown in Fig.10, according to simulation result of circuit S_{12} is below than -21.2dB and it shows good isolation of input and output.

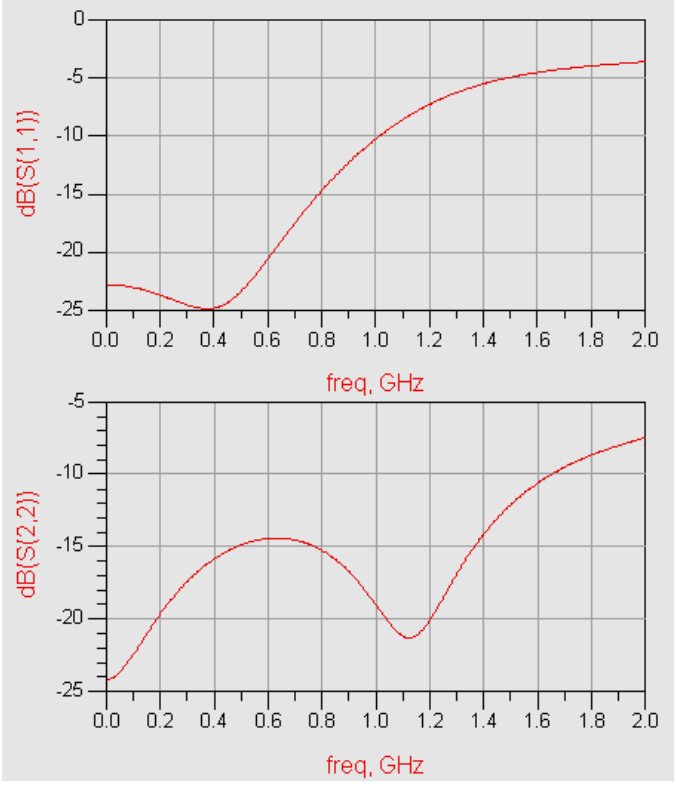

Fig. 9..Input and output matching diagram.

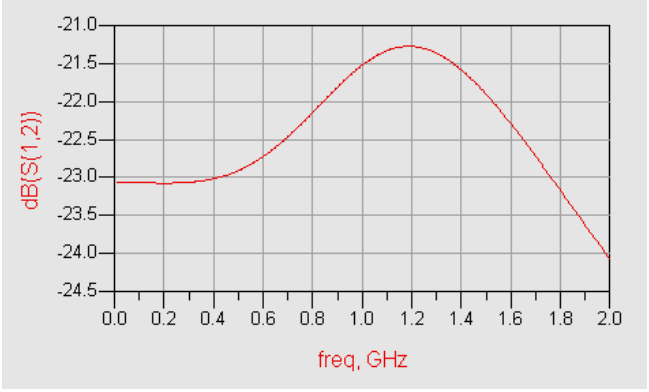

Fig. 10. .S_{12} diagram.

VI. Conclusion

The drain-inductive gain-peaking technique is proposed to improve the gain flatness of the 0.18 m CMOS wideband LNA using shunt-feedback thermal noise cancelling technique. Through the mechanism of pole splitting and frequency pushing, the gain flatness of the amplifier can be enhanced significantly. The wideband CMOS LNA achieves the gain of 17.43 dB with ±0.114dB variation from 50 to 900 MHz. Moreover, the fast gain roll-off outside the desired signal band can help reject jamming and interference.

Under the constraint of low power consumption, the wideband CMOS LNA achieves excellent gain flatness and noise figure.

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