

Semi Empirical Model for MOSFET at Low Temperature for Linear Region Operation

Robin Kumar¹, Manish Hooda³, O.P Sinha²

Department of ECE, Mewar University, Rajasthan, India
Amity Institute of Nanotechnology, Amity University, U.P., Noida- 201303, India
Semiconductor Laboratory, S.A. Nagar, Mohali, India

¹rkumar5@amity.edu

³manisk@scl.gov.in

²sinhaop@gmail.com

Abstract— In the present work a semi-empirical model of Si MOSFET in temperature range of 10k -200k for linear region operation is presented. The Si MOSFET model includes the combined effect of variation in inversion charge (Q_i) and field effect carrier mobility (μ_{FE}) on the current (I) voltage (V) characteristics of Si MOSFET due to low temperature variations. At low temperature due to freeze out effect there remain a fully ionized depletion region beneath the SiO₂ which is responsible for the modification of substrate surface potential (ϕ_s). Further the flat band voltage (V_{FB}) varies with interface trapped charges (Q_{it}) which in turn effect the characteristics of the device. The depletion region charge (Q_{dep}) and inversion region charge (Q_i) are a function temperature as the temperature decreases both ϕ_s and surface depletion edge (X_{dm}) increases which also causes Q_{dep} to decrease. In the calculation of Q_i the variations of Q_{dep} , ϕ_s , Q_{it} and fixed charge (Q_F) are considered.

Keywords – MOSFET, Temperature, Device, semi-empirical

I. INTRODUCTION

Following the Moore's laws, the device geometries has reaches to nano-meter scale regime where second-order effects, like short channel and quantum effect starts dominating and become crucial for device performance [1-2]. However the low temperature operation can be one of the possible solutions to the problems of further scaling down the device. Enhancement of various important parameters such as increase of carrier mobility, low power consumption, a steeper sub threshold slope, a decrease of leakage current, a reduced thermal noise, and an increased thermal conductivity at low temperature has been reported [3,4].

Variation in device parameters due to change in temperature create problems in electronic circuit design

so it is necessary to understand and model the effect of temperature on various device parameters as this facilitates to determine several failure mechanisms in semiconductor devices at different temperatures and help in better high performance circuit designs[5].

This paper presents a semi-empirical model of Si MOSFET in temperature range of 10k -200k for linear region operation is presented. The Si MOSFET model includes the combined effect of variation in inversion charge (Q_i) and field effect carrier mobility (μ_{FE}) on the current (I) voltage (V) characteristics of Si MOSFET due to low temperature variations. The simulated results are compared with experimentally measured characteristics of a conventionally fabricated N MOS device.

II. MOSFET MODEL

The linear region of N MOSFET is expressed by [7]

$$I_d = \frac{W}{L} Q_i \cdot \mu_{eff} \cdot V_d \quad (1)$$

Where Q_i inversion layer charge, V_d drain current and μ_{eff} is effective mobility. Field effect mobility μ_{FE} is expressed by equation (2).

$$\mu_{FE} = \frac{L \cdot gm}{w \cdot Cox \cdot V_d} \quad (2)$$

Transconductance (gm) is given by

$$gm = \frac{dI_d}{dV_G} \quad (3)$$

The I -V characteristics can be obtained by knowing the value of inversion layer charge (Q_i) and effective mobility (μ_{eff}).

A. The Temperature Dependence of Inversion Charge

The inversion charge (Q_i) is function of temperature and other factors and can be approximated by equation (4). [6]

$$Q_i = \frac{\epsilon_s K T N_A(x_{dm})}{Q_{dep}} \cdot e^{(\beta \cdot \phi_s - \beta \cdot \phi_{s0})} \quad (4)$$

Where ϕ_s substrate surface potential, x_{dm} substrate depletion edge, ϕ_{s0} substrate surface potential at the onset of the inversion and β is an empirical value. As the temperature decrease both the ϕ_s and x_{dm} increase that lead to increase in Q_{dep} . Which is quite less than the Q_i . In linear region the equation (4) can be modified as

$$Q_i = \frac{\epsilon_s K T N_A(x_{dm})}{Q_{dep}} \cdot e^{(\beta \cdot \phi_s)} \quad (5)$$

Applied gate voltage V_G is given by the charge conservation equation (6)

$$V_G = V_{FB} + \phi_s + \frac{Q_m + Q_{dep} + Q_{it} + Q_F + Q_m}{C_{ox}} \quad (6)$$

Where Q_{it} is interface trapped charge, Q_F is fix charge (oxide) and Q_m is mobile charge and C_{ox} is oxide capacitance.

B. Mobility Modeling

Mobility is a function of inversion layer charge Q_i and below 40K the μ_{eff} (effective mobility) exhibit bell shaped behavior with inversion charge [7-10]. The effective mobility and field effect mobility is given by equation (7) and (8)

$$\mu_{eff} = \frac{2 \mu_m}{\frac{Q_i}{Q_m} + \frac{Q_m}{Q_i}} \quad (7)$$

$$\mu_{FE} = \frac{2 \mu_{eff}^2}{\mu_m} \quad (8)$$

Where μ_m is the maximum effective mobility and Q_m is the corresponding charge.

C. 2.3 Depletion charge Model

The depletion charge and substrate surface potential is given by equation (9) and (10). [11]

$$Q_{dep} = \int_0^{x_{dm}} q \cdot N_A(x) dx \quad (9)$$

$$\phi_s = \frac{q}{\epsilon_s} \int_0^{x_{dm}} q \cdot N_A(x) dx \quad (10)$$

III. RESULTS

Figure 1 shows the transfer characteristics of MOSFET model in the weak inversion region. The experimental and theoretical characteristics are quite close.

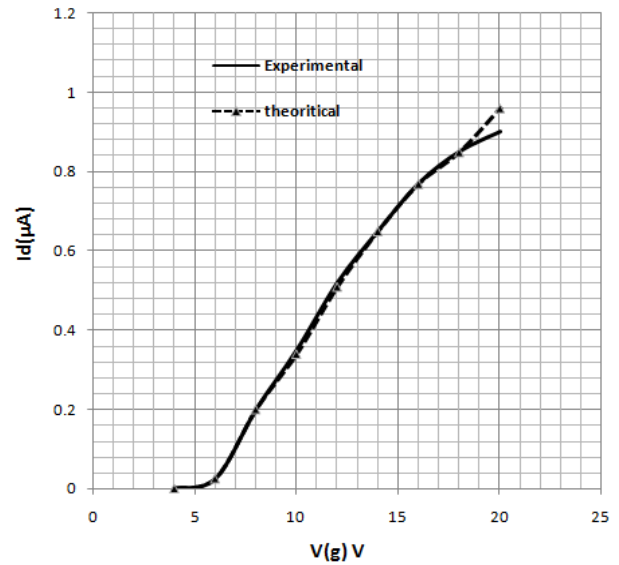


Fig 1. Variation of $I(d)$ Vs $V(g)$ in weak inversion region with $V(d)=60mV$, $W/L=1$ and temperature $=20K$.

IV. CONCLUSION

A semi empirical model for N channel MOSFET for linear region is presented. The model predicts good transfer characteristics of N channel MOSFET at low temperature.

REFERENCES

- [1] R. Murali, B. L. Austin, L. Wang, and J. D. Meindl, "Short-channel modelling of bulk accumulation MOSFETs," IEEE Trans. Electron Devices, vol.51, no.6, pp.940-947, June 2004.
- [2] V. P. Trivedi and J. G. Jerry, "Quantum-mechanical effects on the threshold voltage of undoped double-gate MOSFETs," IEEE Electron Device Lett., vol.26, no.8, pp.579-582, August 2005. H. Poor, *An Introduction to Signal Detection and Estimation*. New York: Springer-Verlag, 1985, ch. 4.

- [3] B. Yu, H. Wang, C. Riccobene, H. S. Kim, Q. Xiang, M. R. Lin, L.Chang, and C. Hu, "Nanoscale CMOS at low temperature: design, reliability, and scaling trend," VLSI Tech. Symp., pp.23-25. April 2001
- [4] Low Temperature CMOS-A Brief Review
William F. Clark, Badih El-Kareh, Renato G. Pires, Stephen L. Titcomb, *IEEE*, and Richard L. Anderson, *IEEE Transactions On Components, Hybrids, And Manufacturing Technology*, Vol. 15, No. 3, June 1992
- [5] An Investigation Of Mosfet Statistical And Temperature Effects, J.A. Power, R. Clancy, W. A. Wall, A. Mathewson, and W.A. Lane Roc. *IEEE 1992 Int Conference on Microelectronic Test Structures*, Vol5, March 1992.C. J. Kaufman, Rocky Mountain Research Lab., Boulder, CO, private communication, May 1995.
- [6] The Temperature-Dependence Of Threshold Voltage Of N-Mosfets With Nonuniform Substrate Doping H. H. CHEN, S. H. TSENG and J. GONG, *Solid-State Electronics* Vol. 42, No. 10, pp. 1799-1805, 1998M. Young, *The Technical Writers Handbook*. Mill Valley, CA: University Science, 1989.
- [7] Modeling Of Ohmic MOSFET Operation At Very Low Temperature. G. Ghibaud, F. Balestra. *Solid state Electronics*, Vol. 31. No.1. pp 105-108, 1988 S. Chen, B. Mulgrew, and P. M. Grant, "A clustering technique for digital communications channel equalization using radial basis function networks," *IEEE Trans. Neural Networks*, vol. 4, pp. 570-578, Jul. 1993.
- [8] G. Ghibaud, *J.Phys.* 19C, 767, 1998.
- [9] F.F. Fang , A.B. Fowler, *Phys.Rev.* 3,619 (1968).
- [10] A.Yagi, S. Kawajii, *Appl.Phys Lett.*33,349(1978)
- [11] Marshak,A.R., *IEEE Trans. Electron Device.*, 1983,26,361-364.