

Low Power Flash ADC

#¹M.Subba Reddy, #²C.Md.Asalam

#¹Department of Electronics and Communication Engineering
#²Vaagdevi Institute of Technology & Science, JNT University, Kadapa, India

¹subbareddy463@gmail.com

²aslam_c73@rediffmail.com

Abstract—In this paper, a new design for a low power CMOS flash Analog-to-Digital Converter (ADC) is proposed. A 6-bit flash ADC, with a maximum acquisition speed of 1GHz, is implemented in a 1.2 V analog supply voltage. HSpice simulation results for the proposed flash ADC verifying the analytical results are also given. It shows that the proposed 6-bit flash ADC consumes less power in a commercial 90nm process. The new design offers lower number of comparators and lower power consumption compared with the traditional flash ADC.

Keywords:-90nm cmos;low power; sampling rate; resolution;

I. INTRODUCTION

Analog-to-Digital Converters (ADCs) are useful building blocks in many applications such as a data storage read channel and an optical receiver because they represent the interface between the real world analog signal and the digital signal processors. Many implementations have been reported in the literature in order to obtain high-speed analog-to digital converters (ADCs). Among those realizations are the ones that are based on flash architecture which have received a great interest since they offer a high sampling frequency and a high conversion speed because of its fully parallel architecture. The main problem of this kind of architectures is that they consume much power and the complexity of the design increases proportionally with the resolution. Successive approximation architectures which have a logarithmic dependence on resolution are alternative approaches to reduce the complexity and the power consumption of flash ADC. On the other hand, it's not desirable to use those kinds of ADCs in high-speed applications since they consume multiple clock cycles to implement the conversion algorithm, which needs more time interleaving to increase the conversion speed. The main concern of this paper is to reduce the power consumption for flash ADC to be suitable for usage in low Voltage applications. We present a new low power 6-bit flash ADC which uses minimum number of comparators. The new design uses 10 comparators and 9 multiplexers while the traditional one uses 63 comparators. The rest of the paper is organized as

follows. Section II reviews the traditional flash architecture. Section III describes the proposed 6-bit flash ADC. Section IV provides the simulation results

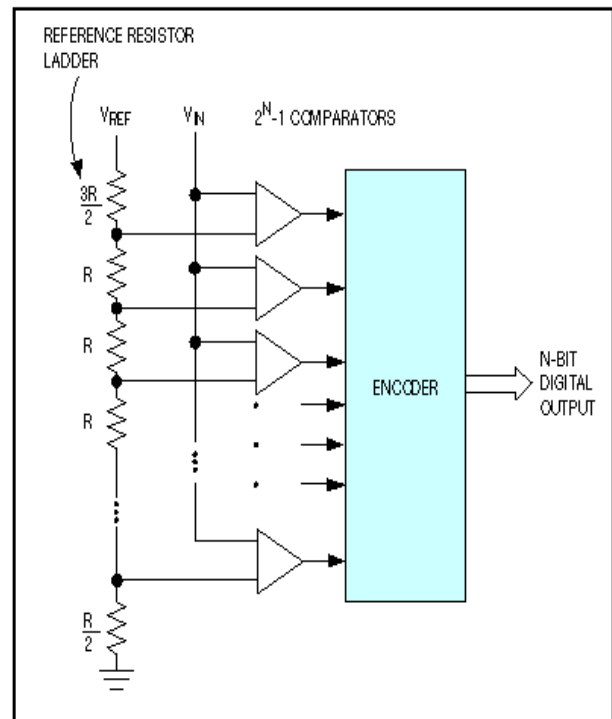


Fig. 1 Block diagram of n-bit Flash ADC architecture

II. FLASH ADC ARCHITECTURE

Fig 1 shows a block diagram of n-bit flash ADC. The reference voltage is subdivided in a set of 2^n reference voltages. These voltages are compared with the analog input signal in just one clock cycle. The encoder is used to convert the thermometer code, generated by the comparators, into a binary code that approximates the input signal. The major disadvantage is that the number of the required comparators depends exponentially on the resolution. This dependence leads to high power consumption and large die area. This problem restricts using the flash ADC on low-bit resolution.

III. PROPOSED 6-BIT FLASH ADC

The new Flash ADC is used to minimize the power consumption and the die area. This design requires only 10 comparators and 9 multiplexers to generate the required binary code as shown in Figure 2. In the first step, the input analog signal is compared with half of the reference voltage ($0.5 V_{ref}$) to generate the most significant bit Z_5 . Other fractions of the reference voltage; $0.75V_{ref}$ and $0.25 V_{ref}$; are used as inputs to a multiplexers controlled by Z_5 and the output is compared with the input analog signal to generate the second most significant bit Z_4 . If Z_5 is high then the multiplexer will pass $0.75 V_{ref}$. If not, it will pass $0.25 V_{ref}$. The two most significant bits will be used as control signals to a multiplexer, which have inputs connected to the proper fractions of the reference voltage. The multiplexer will pass the correct fraction which will be compared to the analog signal to generate the next most significant bit Z_3 . The three most significant bits are used to control seven multiplexers which are connected to the inverting terminal of the comparators. These comparators have outputs that are encoded into appropriate values that represent the least significant bits Z_2, Z_1, Z_0 as shown in Table 1.

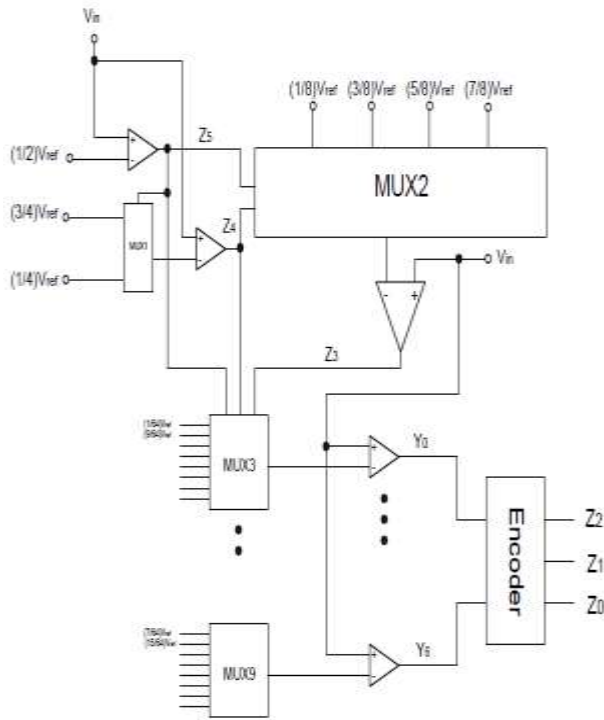


Fig2.The proposed 6-bit flash ADC architecture

TABLE I
CORRESPONDANCE BETWEEN THERMOMETER CODES AND BINARY CODES

Thermometer Code							Binary Code		
Y6	Y5	Y4	Y3	Y2	Y1	Y0	Z2	Z1	Z0
x	x	x	x	x	x	0	0	0	0
x	x	x	x	x	0	1	0	0	1
x	x	x	x	0	1	x	0	1	0
x	x	x	0	1	x	x	0	1	1
x	x	0	1	x	x	x	1	0	0
x	0	1	x	x	x	x	1	0	1
0	1	x	x	x	x	x	1	1	0
1	x	x	x	x	x	x	1	1	1

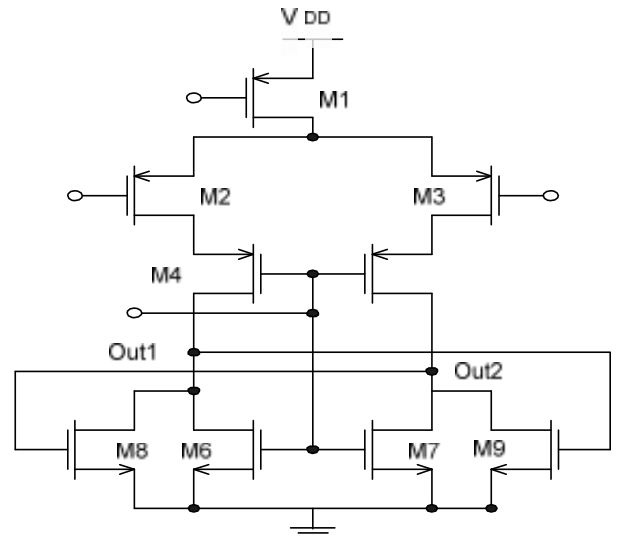


Fig 3(a). CMOS latch schematic

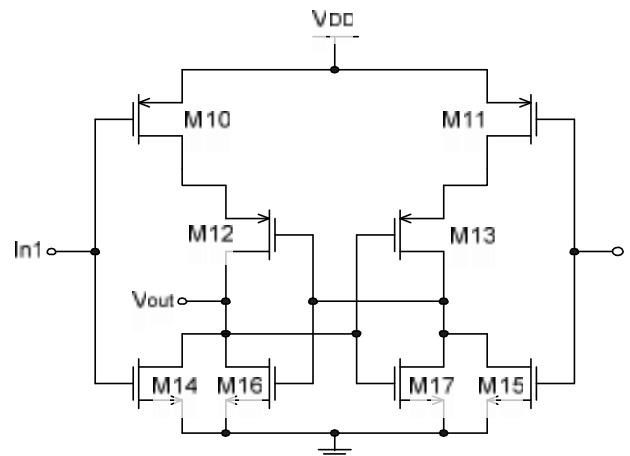


Fig 3(b). SR latch schematic

The main part of any ADC architecture is the

CMOS comparator. In this paper, we use the comparator presented in .It consists of two parts, the CMOS latch and SR latch as shown in Figure 3(a) and Figure 3(b) respectively. There is no separate pre-amplifier in this design. The CMOS latch circuit includes the biasing part, differential and regeneration part. The amplification is done by the PMOS differential pairs. Note that the PMOS transistor sizing can have significant effect on the comparator performance. Increasing the W/L ratio of PMOS transistors {M1-M3} will produce a large current which will cause either M8 or M9 to saturate for a small difference of input voltage (V_{in} and V_{ref}). In this way the offset error can be reduced .If the current difference between M2 and M3 is too large, NMOS transistors will not be able to drive the SR latch for noticeable time and SR latch will be disabled before the regeneration happens. PMOS transistors M4 and M5 are controlled by the clock and act as cascade device. These cascade transistors help to minimize the kick back effect by separating the inputs from the outputs during the regeneration process. On the other hand, the basic function of the SR latch is to act as memory that keeps values for a whole clock period. It may also add some gain to the outputs. The latch provides an interface between analog and digital levels since the outputs of the comparator are digital. Otherwise if analog inputs are connected directly to the digital levels (the comparator outputs), the system becomes unstable. The digital levels can change quite much and can produce bounces even due to small noise spikes.

IV. SIMULATION RESULTS

The proposed ADC has been implemented in a commercial 90nm technology and simulated using Cadence Spectre simulator. The supply voltage used is 1.2V, the reference voltage $V_{ref}=1V$ and the sampling rate is 1 GHz. The comparison of the proposed ADC with related works is shown in Table 1. Figure 4 shows the simulation results of the used comparator when the input voltage is a sinusoidal signal with 20 MHz and figure 5 shows the results of the full architecture sampled at 1 GS/s. The power consumption was optimized to a low value of 23 mW. . Here we are using 90nm CMOS technology. If we reducing the technology further more that is 65um or less the circuit complexity should be reduced as well as the power consumption also reduced. If we see the table II for 160nm technology the power consumption is 160mW.And for 250nm technology the power consumption is 600mW.That is for higher technology the power consumption is also more. Power consumption, all the results are shown in Table II.

TABLE III
COMPARISONS OF FOUR DIFFERENT ADC'S

Design	Existing technologies			This work
	180nm	130nm	250nm	
Technology	180nm	130nm	250nm	90 nm
Sampling Rate (GS/s)	1.2	1.2	1.3	1
Resolution	4-bit	6-bit	6-bit	6-bit
Input range	0.5 V	1 V	1 V	0.6 V
Power Consumption	86 mW	160 mw	600 mW	72 mW

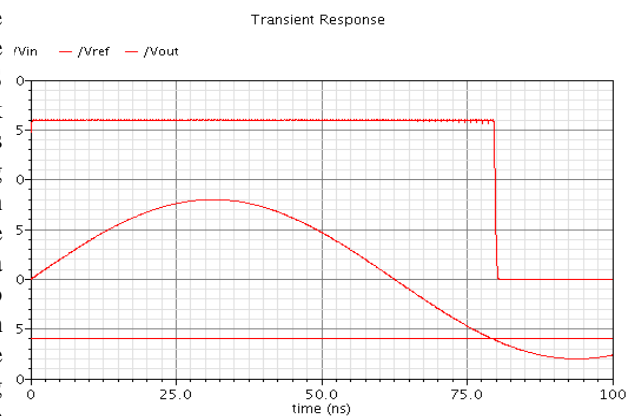


Fig 4. The simulation results of the comparator.

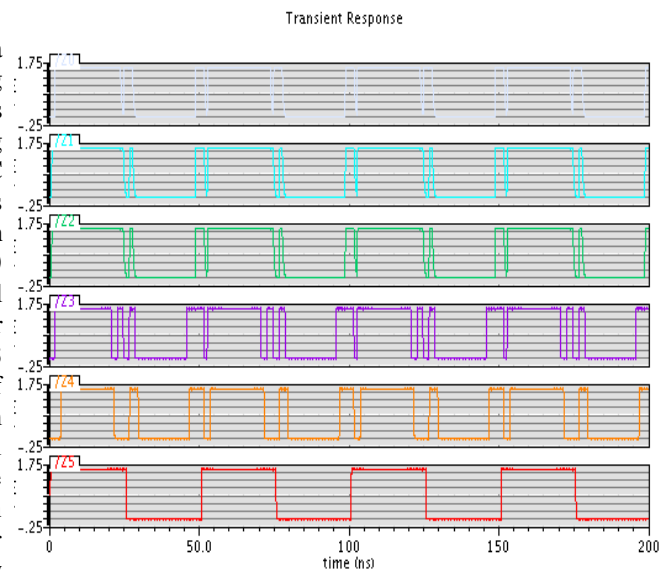


Fig 5. The simulation results of the proposed flash ADC
(V_{in} = 20 MHz sine wave)

V. CONCLUSION

In this paper, the design and the simulation results of a low-voltage 6-bit CMOS ADC has been presented. The maximum sampling speed is 1 GHz and the analog supply voltage is only 1.2V. This architecture can be extended to high resolution applications because of the simplicity of the circuit.

REFERENCES

- [1] K. Nagaraj, D. A. Martin, M. Wolfe, R. Chattopadhyay, S. Pavan, J. Cancio, and T. R. Viswanathan, "A dual-mode 700-Msamples/s 6 bit 200-Msamples/s 7-bit A/D Converter in a 0.25- μ m digital CMOS process," *IEEE J. Solid State Circuits*, vol. 35, no. 12, pp. 1760–1768, Dec. 2000.
- [2] J. Lee, P. Roux, U.-V. Koc, T. Link, Y. Baeyens, and Y.-K. Chen, "A 5-b 10-GSample/s A/D converter for 10-Gb/s optical receivers," *IEEE J. Solid-State Circuits*, vol. 39, no. 10, pp. 1671–1679, Oct. 2004.
- [3] S. Park, Y. Palaskas, and M. P. Flynn, "A 4 GS/s 4b flash ADC in 0.18 μ m CMOS," in *IEEE ISSCC Dig.*, 2006, pp. 570–571, 674.
- [4] R. Kanan, F. Kaess, and M. Declercq, "A 640 mW high accuracy 8-bit 1 GHz flash ADC encoder," in *Proc. IEEE Int. Symp. Circuits and Systems (ISCAS)*, 1999, pp. 420–423.
- [5] J. Sauerbrey, D. Schmitt-Landsiedel, and R. Thewes, "A 0.5V, 1mW Successive Approximation ADC," *Proc. 28th Euro. Solid State Circuits Conf.*, September 2002, Firenze, pp. 247–250.
- [6] S. Mortezaipour and E. K. F. Lee, "A 1-V, 8Bit Successive Approximation ADC in Standard CMOS Process", *IEEE J. Solid-State Circuits*, vol.35, No.4, pp.642–646, April 2000.
- [7] LE, H.P., Zayegh, A., and Singh, J. "A high- speed low-power CMOS comparator with 10- bits resolution,". *Proc. 4th Int. Conf on Modeling and Simulation, MS'02*, Melbourne, Australia, pp. 138-142, March, 2003.
- [8] H.P. Le, A. Zayegh and J. Singh, "Performance analysis of optimized CMOS comparator", *IEEE E. Letters*, Vol. 39, Issue 11, pp. 833 – 835, 2003.
- [9] R. Blazquez, P. P. Newaskar, F. S. Lee, A. P. Chandrakasan, "A baseband processor for impulse ultra-wideband communications," *IEEE Journal of Solid-State Circuits*, Vol. 40, No. 9, pp. 1821–1828 Sept. 2005.
- [10] Christoph Sandner, Martin Clara, Andreas Santner, Thomas Hartig, and Franz Kutter, "A 6bit, 1.2Gs/s Low-Power Flash-ADC in 0.13- μ m Digital CMOS", *IEEE Journal of Solid-State Circuits*, Vol. 40, No. 7, pp. 1499–1505, Jul. 2005.
- [11] K. Uyttenhove, M. S. J. Steyaert, "A 1.8V 6-Bit 1.3-GHz Flash ADC in 0.25- μ m CMOS," *IEEE Journal of Solid-State Circuits*, Vol. 38, No. 7, pp. 1115–1122, Jul. 2003.