IJCAES
ISSN: 2231-4946
Volume III, Special Issue, August 2013

International Journal of Computer Applications in Engineering Sciences
Special Issue on National Conference on Information and Communication (NCIC'13)
www.caesjournals.org

Low Cost Nonrecursive Digital Filter Structures

G. Shanmugaraj[1], N. Kalaiarasi[2]

[1]*Research Scholar, Faculty of Electrical Engg., Anna university, Chennai, INDIA,gsraj76@gmail.com*
[2]*Professor & Head, Dept. of EEE, RMK College of Engg. & Technology, Puduvoyal, Tiruvallur Dt., INDIA, kalaiarasipol_n69@yahoo.co.in*

Abstract—This paper presents a novel method of hardware reduced fast FIR filter structure for parallel data processing.In general, arithmetic operation modules such as adder and multiplier modules, consume much power, energy, and circuit area. The power consumed by the adder structure is also very significant while designing a low power filter. The proposed low power multipliers and low power adders are used to reduce dynamic power consumption of digital FIR filter. Supported by a review of literature, the proposed methodology is superior and economical. The results show improved performance in terms of cost reduction, which has practical implications in terms of applications

Keywords— FIR filter design, FDA Tool, Low Power VLSI

I.INTRODUCTION

Finite impulse response (FIR) filters are widely used in various DSP applications. In some applications, the FIR filter circuit must be able to operate at high sample rates, while in other applications, the FIR filter circuit must be a low-power circuit operating at moderate sample rates. The low-power or low-area techniques have been developed specifically for digital filters. Block (or Parallel) processing can be applied to digital FIR filters to either increase the effective throughput or reduce the power consumption of the original digital filter.

Digital signal processing (DSP) is used in wide range of applications such as telephone, radio, video etc. Most of DSP computations involve the use of multiply accumulate operations (MAC) and therefore the design of fast and efficient multiplier imperative. The demand for portable applications of DSP architectures has dictated the need for low power designs [1]. More over Digital Finite Impulse Response filter has a lot of arithmetic operations. In general, arithmetic operation modules such as adder and multiplier modules have consume much power, energy, and circuit area. Input bit width of the modules is important design parameter for low power. The power digital FIR filter circuit is reduced by optimization of taps and bit width of input signal with filters coefficients. Block processing can be applied to digital FIR filters to either increase effective throughput or reduce the power consumption of filter [5]. The rest of paper is structured as follows. Section II gives summary of FIR filter theory, and section III presents the architectures used in our implementation. Section IV gives Result and comparison of implementing architectures. Section V provides conclusion of the paper.

II FIR FILTER THEORY

Digital filters are very important part in digital signal processing. Filters have two uses, one is signal restoration and other is signal separation. Signal separation is needed when the signal has been contaminated with noise or some other signals. Signal restoration is used when the signal has been distorted in some way. The most commonly used digital filter is linear time invariant filter. In general filtering is described by simple convolution operation as where is input signal, is convolved output and is filter impulse response. Digital filters are two types: Finite Impulse Response (FIR) filters and Infinite Impulse Response (IIR) filters. The filters designed by using finite number of samples of impulse response are called Finite Impulse Response filters. The filters designed by considering all infinite samples of impulse response are called Infinite Impulse Response Filters. Communication

systems for applications such as channelization, channel equalization, matched filtering, and pulse shaping, due to their absolute stability and linear phase properties. The filters employed in mobile systems must be realized to consume less power and operate at high speed. Recently, with the advent of software defined radio (SDR) technology, Finite Impulse Response (FIR) filter research has been focused on reconfigurable realizations. The complexity of the FIR filter is mainly based on the complexity of the coefficient multiplication. Generally the N-tap FIR filter which can be expressed as y(n)=h(n)*x(n)

$$y(n)=\sum_{i=0}^{N-1} h(i)\, x(n-i) \;\; ; n=0,1,2,\ldots\ldots\infty \qquad (1)$$

Where {h(n)} having FIR filter coefficients of length N and {x(n)} is an infinite length input sequence. The polyphase decomposition can be derived from L-parallel FIR filters by decomposing X(Z), Y(Z) and H(Z) into L subsequences as : *Y(Z)=X(Z)H(Z)*

III. MULTIPLIER DESIGN

It is well-known that the application of Block processing to a FIR filter can increase the throughput of the FIR filter. If an L parallel filter is operated at the same clock rate as the original filter, L output samples are generated every clock cycle compared to the single output sample that is produced every clock cycle in the original filter. This implies that the L-parallel filter effectively operates at L times the rate of the original FIR filter. While it is clear that Block processing can increase the throughput of the FIR filter.

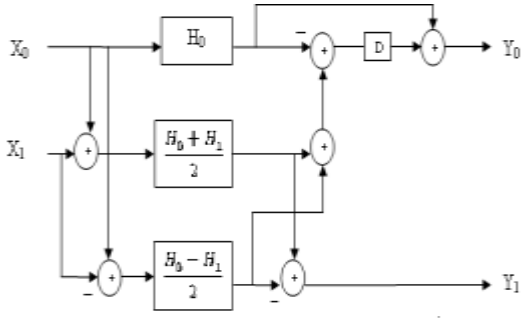

Fig 1: proposed two parallel fast fir filter structure

$$Y_0 = H_0 X_0 + Z^{-2}\{\tfrac{1}{2}[\,(H_0+H_1)(X_0+X_1) + (H_0-H_1)(X_0-X_1)\,] - H_0 X_0\}$$
$$Y_1 = \tfrac{1}{2}[(H_0+H_1)(X_0+X_1) - (H_0-H_1)(X_0-X_1) \qquad (2)$$

The 2 parallel fast FIR filtering structure which results from this (2-by-2 Poly Phase Decomposition**)** FFA is shown in Fig. 1.This structure computes a block of 2 outputs using 3 length-N/2 symmetric coefficients FIR filters and 6 pre / post processing additions.

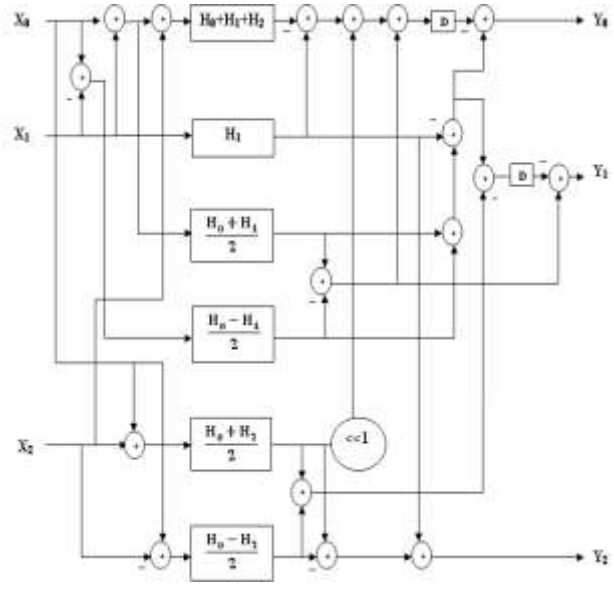

Fig. 2: Proposed Three parallel Fast FIR Filter structure

$$Y_0 = \frac{1}{2}[(H_0+H_1)(X_0+X_1) + (H_0-H_1)(X_0-X_1) - H_1X_{1]} - Z^{-3}\{\frac{1}{2}[(H_0+H_1)(X_0+X_1) - (H_0-H_1)(X_0-X_1)] + H_1X_1 + (H_0+H_2)(X_0+X_2) - (H_0+H_1+H_2)(X_0+X_1+X_2)\}$$

$$Y_1 = \frac{1}{2}[(H_0+H_1)(X_0+X_1) - (H_0-H_1)(X_0-X_1)] - Z^{-3}\{\frac{1}{2}[(H_0+H_1)(X_0+X_1)+(H_0-H_1)(X_0-X_1)] - \frac{1}{2}[(H_0+H_2)(X_0+X_2) + (H_0-H_2)(X_0-X_2)] - H_1X_1\}$$

$$Y_2 = \frac{1}{2}[(H_0+H_2)(X_0+X_2) - (H_0-H_2)(X_0-X_2)] + H_1X_1$$

The 6 parallel FIR filter is generated by cascading a (2-by-2) FFA with a (3-by-3) FFA. The process is essentially identical to the process that was used to generate the 4-parallel filtering structure.

IV EXPERIMENTAL RESULTS

Table I shows the summary of proposed FIR filter structure for hardware saving in terms of percentage. This effective designing structure has reduced the hardware cost considerably. For example, four parallel FIR filtering structure can save up to 2N/8 multiplications for implementation. The infinite precision coefficients were generated using the Remez function in MATLAB. If the phase of the filter is linear, the symmetrical architecture can be used to reduce the multiplier operation. Many algorithm transformation techniques are available for optimum implementation of the digital signal processing algorithms. Reducing the implementation area is important for complex algorithms,

The cascading of FFAs is a straight-forward extension of the original FFA application. For example, a (p-by-p) FFA can be cascaded with a (q-by-q) FFA to produce a (p **x** q)-parallel filtering structure. The set of FIR filters that result from the application of the (*p-by-p)* FFA are further decomposed, one at a time, by the application of the (q-by-q) FFA. The resulting set of filters will be of length N/(p x *q).* When cascading the FFAs, it is important to keep track of both the number of multipliers and the number of adders required for the filtering structure.

Fig : 3 Four Parallel FIR Filter RTL Diagram

Table 1:Summary of proposed results for saving Multiplications

N-TAP	L= 2	L= 4	L= 8	N-TAP	L= 3	L= 6
24	20%	7%	21.1%	27	17.4%	19.8%
72	20%	13.9%	18.9%	81	19.1%	17.2%
144	20%	13.0%	19.5%	147	13.2%	16.4%
576	20%	11.9%	13.7%	591	19.8%	17%

V. CONCLUSION

In this paper a low power and low area digital FIR filter is presented. In this paper we have proposed an algorithm for reducing the hardware complexity of linear phase FIR digital filters without resorting to increasing the adder depth. The proposed FIR filters have been synthesized and implemented using Xilinx tools and power analyzed using Xilinx Xpower analyzer.

REFERENCES

[1] J. G. Chung and K. K. Parhi, *"Frequency-spectrum-based low-area low-power parallel FIR filter design," EURASIP J. Appl. Signal Process.*, vol. 2002, no. 9, pp. 444–453, 2002.

[2] K. K. Parhi, *VLSI Digital Signal Processing Systems: Design and Implementation.*New York: Wiley, 1999.

[3] D. A. Parker and K. K. Parhi, *"Low-area/power parallel FIR digital filter implementations," J. VLSI Signal Process. Syst.*, vol. 17, no. 1, pp. 75–92, 1997.

[4] C. Cheng and K. K. Parhi, *"Low-cost parallel FIR structures with 2-stage parallelism," IEEE Trans. Circuits Syst. I, Reg. Papers*, vol.54, no. 2, pp. 280–290, Feb. 2007.

[5] Z.-J. Mou and P. Duhamel, *"Short-length FIR filters and their use in fast nonrecursive filtering," IEEE Trans. Signal Process.*, vol. 39, no.6, pp. 1322–1332, Jun. 1991.

[6] J. I. Acha, *"Computational structures for fast implementation of L-path and L-block digital filters," IEEE Trans. Circuit Syst.*, vol. 36, no. 6, pp. 805–812, Jun. 1989.

[7] C. Cheng and K. K. Parhi, *"Hardware efficient fast parallel FIR filter structures based on iterated short convolution*," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 8, pp. 1492–1500, Aug. 2004.

[8] C. Cheng and K. K. Parhi, *"Furthur complexity reduction of parallel FIR filters*," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS 2005)*, Kobe, Japan, May 2005.

[9] I.-S. Lin and S. K. Mitra, *"Overlapped block digital filtering," IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 43, no. 8, pp. 586–596, Aug. 1996.

[10] *"Design Compiler User Guide,"* ver. B-2008.09, Synopsys Inc., Sep.

[11] H. K. Kwan and M. T. Tsim. *High speed 1-D FIR digital filtering architectures using polynomial convolution.* In *Proceedings of IEEE International conference on Acoustics,*

[12] R. E. Blahut, *Fast Algorithms for Digital Signal Processing*. Reading,MA: Addison-Wesley, 1985.

[13] H. J. Nussbaumer, *Fast Fourier Transform and Convolution Algorithms*.Berlin, Heidelberg, New York: Springer-Verlag, 1982.

[14] Y. C. Lm and B. Liu. *Design of cascade form FIR filters with discrete valued coefficients.* IEEE transactions on Acoustics, *Speech,* and Signal Processing, pages 1735-1730, November 1988.

[15] Y. C. Lm and B. Liu. *Design of cascade form FIR filters with discrete valued coefficients.* IEEE transactions on Acoustics, *Speech,* and Signal Processing, pages 1735-1730, November 1988.

[16] Y.-C. Tsao and K. Choi, *"Area-efficient parallel FIR digital filter structures for symmetric convolutions based on fast FIR algorithm." IEEE trans.Very large scale integr.(VLSI) Syst.*, vol. 20, no.2, pp.366-371, Feb.2010.

[17] Y.-C. Tsao and K. Choi, "*Area-efficient VLSI Implementation for Parallel Linear-Phase FIR digital filters s of Odd Length Based on fast FIR algorithm." IEEE trans. . Circuits Syst. II,* vol. 59, no.6, pp.371-375,Jun. 2012.