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Low-Power And Area-Efficient Carry Select Adder Using Modified Bec-1 Converter

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Abstract -**Carry Select Adder (CSLA) is one of the fastest adders used in many data-processing processors to perform fast arithmetic functions. From the structure of the CSLA, it is clear that there is scope for reducing the area and power consumption in the CSLA. This work uses a simple and efficient transistor-level modification in BEC-1 converter to significantly reduce the area and power of the CSLA. Based on this modification 16-b square-root CSLA (SQRT CSLA) architecture have been developed and compared with the SQRT CSLA architecture using ordinary BEC-1 converter. The proposed design has reduced area and power as compared with the SQRT CSLA using ordinary BEC-1 converter with only a slight increase in the delay. This work evaluates the performance of the proposed designs in terms of delay, area, and power by hand with logical effort and through Cadence Virtuoso. The results analysis shows that the proposed CSLA structure is better than the SQRT CSLA with ordinary BEC-1 converter.**

***Keywords*—-** (Binary to Excess-1 converter,Low power,Area Efficient,CSLA)

I. INTRODUCTION

Design of area- and power-efficient high-speed data path logic systems are one of the most substantial areas of research in VLSI system design. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after theprevious bit position has been summed and a carry propagated into the next position.The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum .However,the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by consideringcarry input cin = 0 andcin = 1, then the final sum and carry are selected by the multiplexers (mux).The power and Area of the Carry select Adder can be reduced by using BEC-1 converter instead of Ripple Carry Adder(RCA). The basic idea of this work is to use transistor level modified Binary to Excess-1 Converter (BEC) instead of Ordinary BEC(gate level) with cin = 1 in the CSLA to achieve lower area and power consumption . The main advantage of this transistor level modified BEC-1 comes from the lesser number of MOS transistor than the Ordinary BEC-1.

II. BEC

As stated above the main idea of this work is to use transistor level modified BEC instead of the ordinary BEC with cin=1 in order to reduce the area and power consumption of the CSLA. To replace the n-bit ordinay BEC, an n-bit transistor level modified BEC is required.The function table of a 3-b BEC are shown in Table I.

TABLE-I

FUNCTION TABLE OF THE 3-B BEC

Fig. 1 illustrates how the basic function of the CSLA is obtained by using the 4-bit BEC together with the mux. One input of the 8:4 mux gets as it input (B3, B2, B1, and B0) and another input of the mux is the BEC output. This produces the two possible partial results in parallel and the mux is used to select either the BEC output or the direct inputs according to the control signal Cin. The importance of the BEC logic stems from the large silicon area reduction when the CSLA with large number of bits are designed.

INPUT[0:3]	OUTPUT[0:3]
000	001
001	010
010	011
011	100
100	101
101	110
110	111
111	000

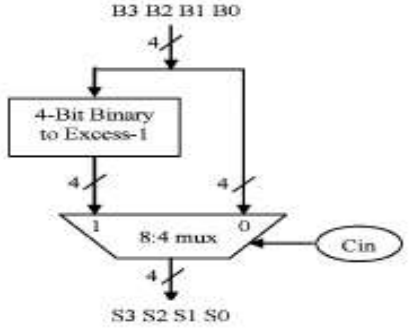

Fig. 1. 4-b- BEC With 8:4 MUX

III. 16-B SQRT CSLA USING ORDINARY BINARY TO EXCESS-1 CONVERTER

The structure of the 16-b SQRT CSLA using ordinay BEC for RCA with cin=1 to optimize the area and power is shown in Fig. 2 We again split the structure into five groups. The Power and area estimation of each group ordinary BEC and Mux are shown in Fig 3

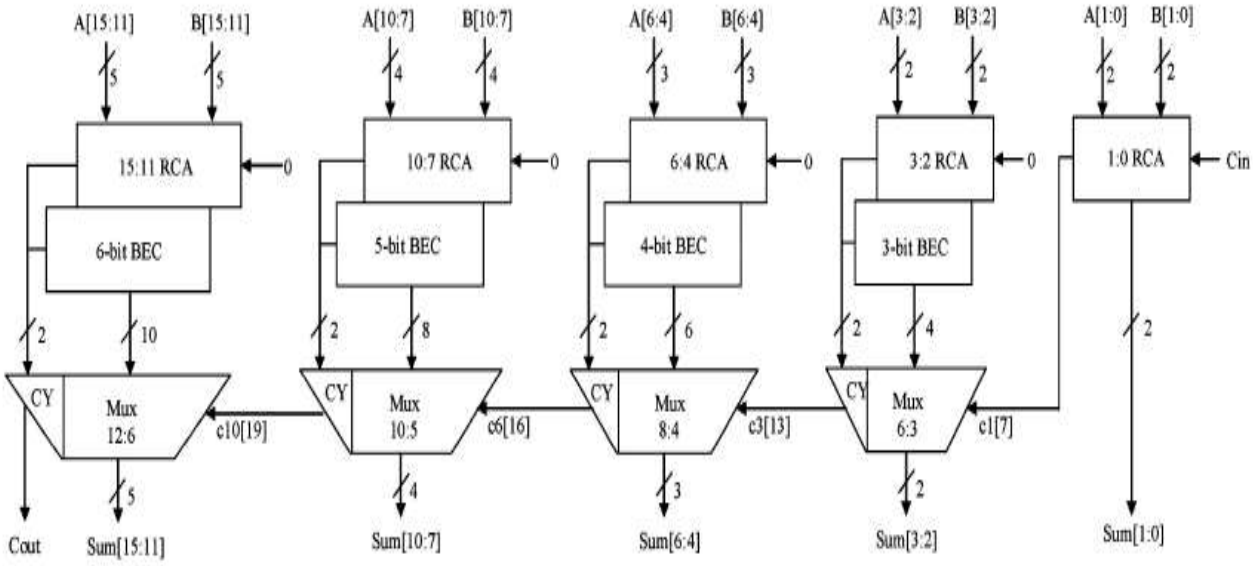

Fig. 2. 16-b SQRT CSLA. The parallel RCA with Cin = 1is replaced with BEC.

1) The Fig. 3 has transistor level design of 3-b BEC and 6:3 Mux.The ordinary 3-b BEC is used in CSLA for reducing the power and area of the adder.The total number of PMOS and NMOS transistor in the 3-b BEC and MUX are 42 and 42.

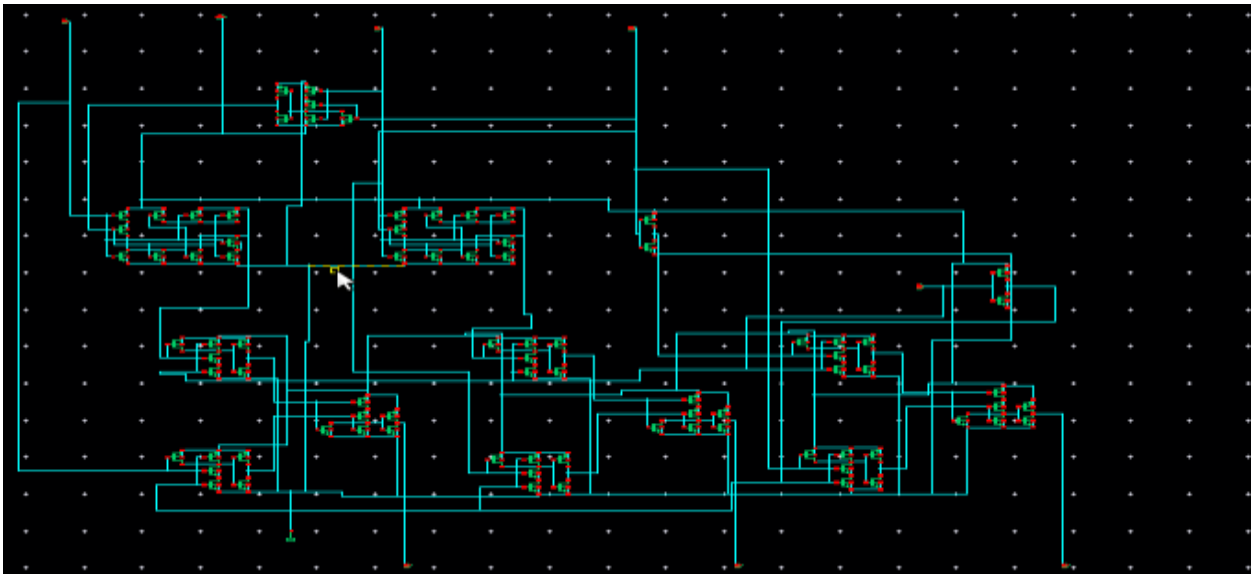

Fig. 3 Transistor level design of ordinary 3-b BEC and 6:3 Mux

Similarly the ordinary 4-b BEC and 8:4 Mux,5-b BEC and 10:5 Mux ,6-b BEC and 12:6 Mux has been designed in transistor level .The Table-II shows the number of Mos transistors required for various bits of BEC and MUX.

TOTAL MOS TRANSISTORS OF ORDINARY BEC AND MUX

Groups	No of PMOS Transistors	No of NMOS Transistors	Total no of MOS Transistors

Group2(3-b BEC and 6:3 mux)	42	42	84
Group3(4-b BEC and 8:4 mux)	59	59	118
Group4(5-b BEC and 10:5 mux)	76	76	152
Group5(6-b BEC and 12:6 mux)	93	93	186
Total no of MOS Transistor	270	270	540

IV. 16-B SQRT CSLA USING TRANSISTOR LEVEL MODIFIED BINARY TO EXCESS-1 CONVERTER

The structure of the proposed 16-b SQRT CSLA using transistor level modified BEC for RCA with cin=1 to optimize the area and power is same as Fig 3.We again split the structure into five groups. The Power and area estimation of each group ordinary BEC and Mux are shown in Fig.4

1) The Fig. 5 has transistor level design of 3-b BEC and 6:3 Mux.The Transistor level modified 3-b BEC is used in CSLA for reducing the power and area of the adder.The total number of PMOS and NMOS transistor in the 3-b BEC and MUX are 34 and 34

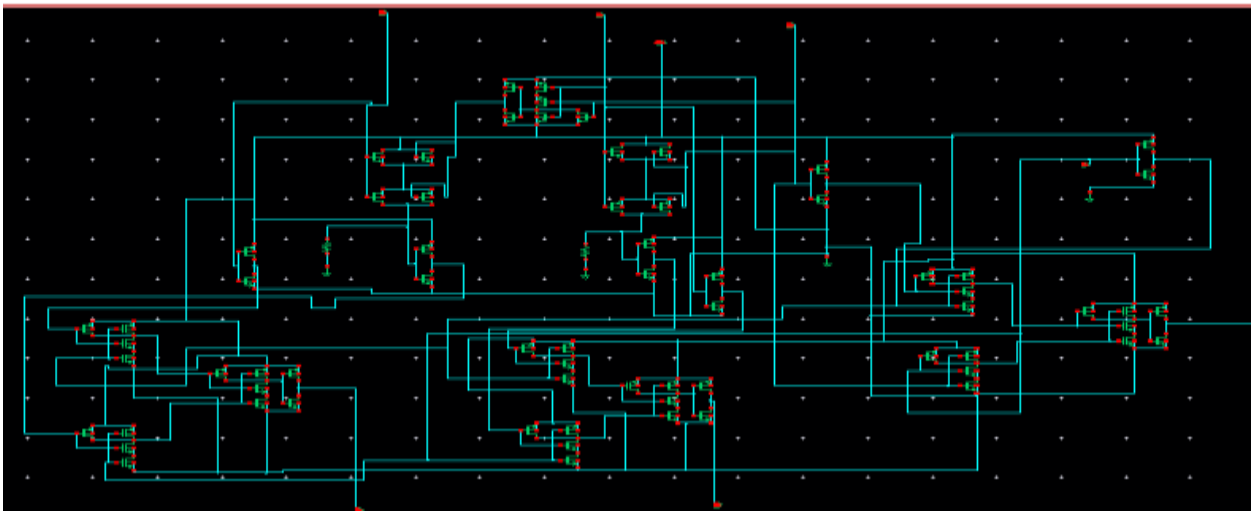

Fig. 4 Transistor level Modified design of 3-b BEC and 6:3 Mux

Similarly the transistor level modified 4-b BEC and 8:4 Mux,5-b BEC and 10:5 Mux ,6-b BEC and 12:6 Mux has been designed.The Table-III shows the number of Mos transistors required for various bits of Modified BEC and MUX.

TOTAL MOS TRANSISTORS OF MODIFIED 3-B BEC

Groups	No of PMOS Transistors	No of NMOS Transistors	Total no of MOS Transistors
Group2(3-b BEC and 6:3 mux)	34	34	68
Group3(4-b BEC and 8:4 mux)	48	48	96

Group4(5-b BEC and 10:5 mux)	62	62	124
Group5(6-b BEC and 12:6 mux)	76	76	152
Total no of MOS Transistor	220	220	440

Comparing Tables II and III, it is clear that the proposed Transistor Level modified BEC and MUX Circuits saves 100 MOS Transistors than the Ordinary BEC and MUX, with only increases in delays.

V. IMPLEMENTATION RESULTS

The design proposed in this paper has been developed using Cadence Virtuoso using typical libraries of gpdk 0.18 um technology.The Current flowing through the circuit can be measured for the input combination .Then the power can be calculated using the current and the voltage required for the the circuit.The similar design flow is followed for both the ordinary BEC-MUX and modified BEC-MUX.

Table IV exhibits the implementations results of both the BEC-MUX structures in terms of delay, area and power. The area indicates the no of MOS transistors used and the total power indicates the maximum power in the circuit. The Delay can be measured in terms of the maximum time taken by the circuit to produce the all outputs for the given inputs.

TABLE-IV

		Area(No of MOS transistors)	Peak current (uA)	Power (mw)	Average Delay (ns)
3-b BEC and MUX	Regular	84	561.269	1.0102	1.066
	Modified	68	485.186	0.8733	0.735
4-b BEC and MUX	Regular	118	737.533	1.3275	1.066
	Modified	96	623.868	1.1229	0.735
5-b BEC and MUX	Regular	152	900.154	1.6202	1.066
	Modified	124	765.430	1.3777	0.735
6-b BEC and MUX	Regular	186	1.05962	1.9073	1.066
	Modified	152	905.330	1.6295	0.735

The reduction in power consumption of modified 3-b BEC-MUX is 13.55%,4-b BEC-MUX is15.41%, 5-b BEC-MUX is 14.97%, and 6-b BEC-MUX is 14.57. The delay overhead for the 3,4,5 and 6-b BEC-MUX circuit is 31.06%

VI. CONCLUSION

A simple approach is proposed in this paper to reduce the area and power of BEC-MUX architecture. The reduced number of transistors of this work offers the great advantage in the reduction of area and also the total power. The compared results show that the modified BEC-MUX has a slightly larger delay (only 31.06%), but the power of the modified BEC-MUX are significantly reduced by 14.70%.The BEC-MUX circuit should be a part of the CSLA.The transistor level modified BEC-MUX circuit can be used in CSLA instead of ordinary BEC-MUX circuit the greater power consumption can be achieved. The modified BEC-MUX architecture is therefore, low area, low power, simple and efficient for VLSI hardware implementation.

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