IJCAES
ISSN: 2231-4946
Volume V, Special Issue, January 2015

International Journal of Computer Applications in Engineering Sciences
Special Issue on International Conference on Computing, Communication and Sensor Network (CCSN-2014)
www.caesjournals.org

8T Double-Ended Read-Decoupled SRAM Cell

Soumitra Pal, Aminul Islam

Electronics and Communication Engineering
Birla Institute of Technology, Mesra
Ranchi, Jharkhand, India, Pin-835215

soumitra10028.13@bitmesra.ac.in, aminulislam@bitmesra.ac.in

***Abstract*-Scaling of SRAM cell beyond 65-nm poses a serious threat to the stability of the cell and is a cause of major concern for the upcoming technologies. Due to random dopant fluctuation (RDF) and other process parameter variations, the cell turns out to be unstable. In this paper, an 8T (8-Transistor) SRAM cell is proposed which offers enhanced data stability during read operation. While reading, the voltage level of the '0' holding node does not increase and thus a near ideal butterfly-curve is achieved, which is crucial to design a robust SRAM cell. In 16-nm technology node, the read static noise margin or read SNM (RSNM) as high as 159 mV at supply voltage (V_{DD}) of 600 mV is achieved by the proposed cell. Therefore, the cell is 4.18× more stable than the standard 6T SRAM cell during read operation and has 1.87× shorter delay than the standard 6T SRAM cell at the same voltage. Also the proposed cell offers 4.15 × improvements in write delay. All these are achieved at a marginal penalty of write static noise margin (WSNM) 1.07× compared to standard 6T.**

***Keywords* -CMOS; Read Delay;Write Delay; Read Stability; Write Ability.**

I. INTRODUCTION

SRAM cell, as specified in the ITRS 2011 (international technology road map for semiconductors) [1] occupies the major portion of the SoC (system on chip) and NoC (network on chip), which made the researchers to scale down the SRAM cell on the basis of layout design rules. Developments had made the technology node scaling below 65-nm, but as we go below 100-nm technology node, stability of the cell is the important concern to be faced by the designers with upcoming technologies. The cell is more susceptible to both Vt (threshold voltage) variations because of channel dopant variation and variations due to device geometry parameters. The atomic level intrinsic variations cannot be eliminated in the manufacturing process [2]. Moreover, SRAM cell is used as cache memory in the microprocessors, high speed SRAM cells should be used to synchronize with the microprocessor. The speed of the SRAM cell can be increased by decreasing the Vt (threshold voltage) of the MOSFET, but decrease in Vt causes leakage current as the limiting factor for the design of the cell. Degradation of SNM during the read operation is a major concern compared. Therefore,there is a need to develop an SRAM cell whose SNM is unaffected by the read operation.

Read failure is more frequent in standard 6T (Fig.1), which is because the node storing '0' is raised to voltage greater than the ground potential, due to the voltage divider developed between the access transistor and the pull down transistor. This may lead to flipping of the stored state if the voltage developed is greater than the threshold voltage of the other inverter (storing '1') in the cross coupled network. Various designs varying from 6T to 13T of the SRAM cells had been proposed. A single ended 6T SRAM cell proposed in [3] reduces the read time but the RSNM (read static noise margin) is not improved. Another single ended 6T

SRAM cell [4] is proposed by A.Islam, et al. This cell improves the power dissipation during both read and write mode at the cost of read/write delay and RSNM. A 7T SRAM cell [5] obtained by adding the extra

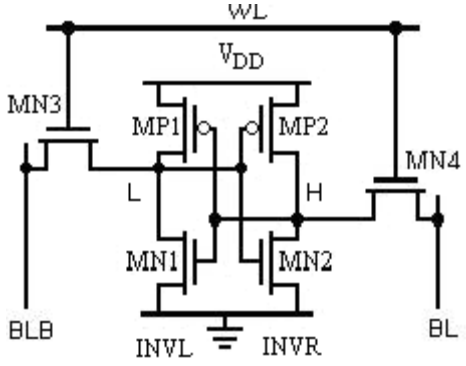

Fig. 1. Standard 6T (STD6T) SRAM Cell

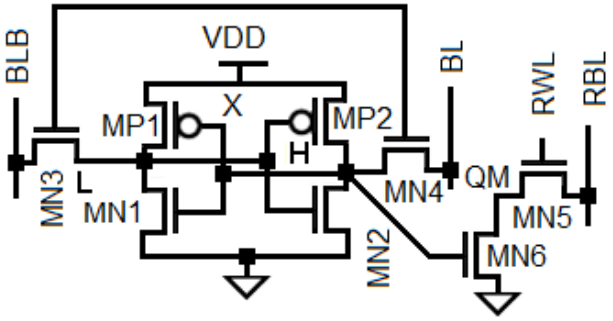

Fig. 2. Single ended read-decoupled 8T SRAM cell [7]

transistor in between the cross coupled inverters could improve read stability and write ability by appropriate transistor sizing. But leakage current and RSNM could not be improved simultaneously.In 8T SRAM cell [6], access transistors of conventional 6T SRAM cell are replaced by the transmission gates, which provide an advantage of higher RSNM with a drawback of longer read delay. Various other 8T and 10T SRAM cells are also proposed to improve the read stability [7]-[10]. These cells improves the read stability by considerable amount, but as these are single ended, these are subjected to a sense margin problem [11]. A 10T SRAM cell [12] was proposed by A. Islam, et al. to minimize the leakage current and the effect of PVT (process, voltage and temperature) variations and to increase the RSNM with a penalty of larger device count. By the same authors in [12] a low-leakage 11T SRAM cell [13] was also proposed, with an advantage of optimized power consumption as compared to conventional 6T at the cost of larger read delay. In 13T SRAM cell [14], RSNM is improved at the expense of lower write ability and larger area consumption.

This paper proposes a double-ended SRAM cell to minimize the difference of speed between the microprocessor and SRAM while maintaining the cell stability. Therefore, an improvement in RSNM is attained in the proposed cell. The proposed cell also offers shorter read and write delay.

HSPICE 16-nm PTM [15] ((developed by the Nanoscale Integrations and Modeling (NIMO) Group at Arizona State University (ASU)) technology is used for simulation and comparison of the proposed cell with the standard 6T (STD6T) STAM cell and single ended read decoupled 8T (SERD) (Fig. 2) cell [7].

Further, the proposed design is explained in Section II. In Section III, simulation results are presented and compared with other two cells. Finally, Section IV concludes the paper.

II. PROPOSED DESIGN

The proposed design (Fig. 4) resembles the standard 6T (STD6T) except that extra transistors are used for read operation. One more transistor is connected at the tail of the cross coupled inverter. One of the extra transistors for read operation, RT (read transistor) and the tail transistor, called write assist transistor, are

made common for entire row (Fig.3). Read buffer is made up of one NMOSFET (RT) and two PMOSFETs (MP3/MP4) (PMOSFETs are used instead of NMOSFETs because PMOSFET shows higher tolerance

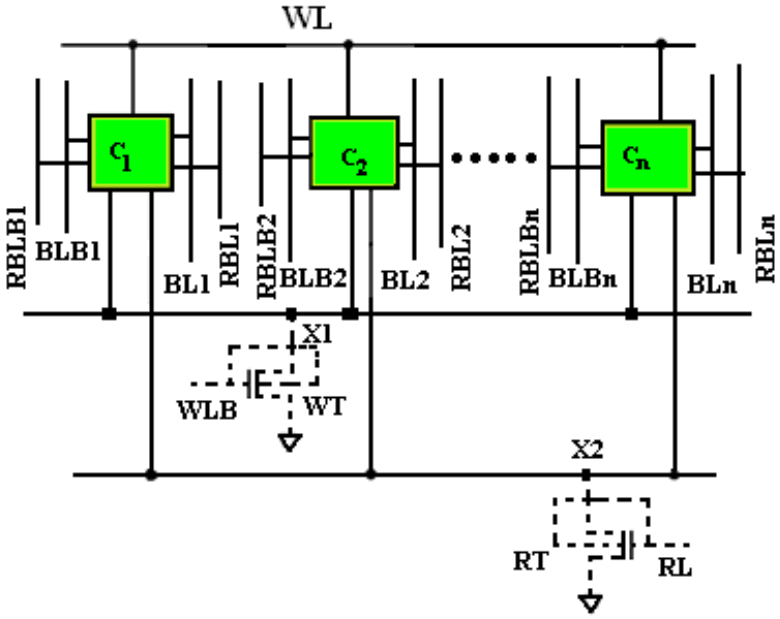

Fig. 3. Proposed Design architecture

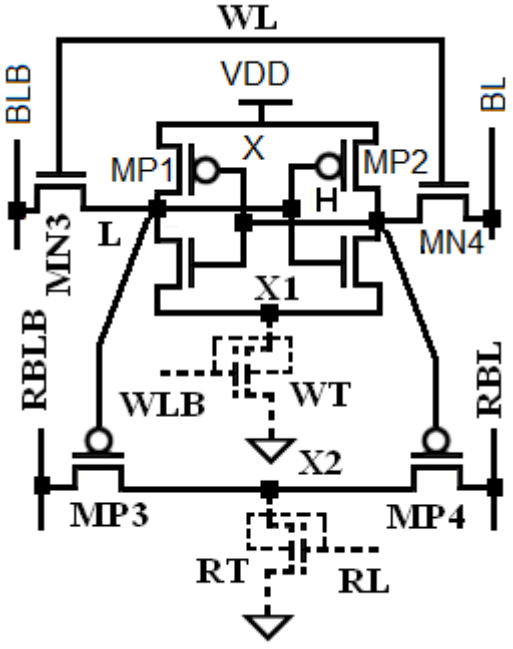

Fig. 4. Proposed Double Ended Read Decoupled (DERD8T) cell

against radiation. There is no effect of radiation bombardment on leakage current in case of PMOS, whereas in NMOS, the leakage current increases [16]).

Moreover, flicker (1/f) noise is lesser in PMOS than that in NMOS transistor. In addition, degradation in mobility of holes is lesser as compared to that of electrons due to comprehensive stress offered by shallow trench isolation (STI).

RSNM is improved, because while read operation the PMOS transistors and the RT (read transistor), decouple the nodes, storing the data. Separate read and write operations are performed in the proposed SRAM cell. RBL (read bitline) and RBLB (read bitline bar) used for read operation, While BL (bitline) and BLB (bitline bar) are used for write operation.

The proposed cell is called double-ended read decoupled 8T (DERD8T), because during read operation it decouples the storage nodes (Fig.3). During read operation RL (read line) is made high and both the read bitlines RBLB and RBL are precharged to the supply voltage. The FETs MP3 or MP4 conducts depending on the storage data, which provide a path for RBLB/RBL to discharge through MP4/MP3 and finally through RT. The cell stability is enhanced as the stored nodes are decoupled during read operation.

III. RESULTS AND COMPARISON

Different important design metrics of an SRAM cell like – read delay, write delay, RSNM and WSNM of the proposed DERD8T and standard 6T cell are estimated and compared with STD6T and SERD8T in the following subsection.

A. Read Delay Analysis

In case of the read operation, both the read bitlines, RBL and RBLB, are precharged to the supply voltage. Read line (RL) is connected to VDD and word line (WL) is made low. As WL is made low WLB (complement of WL) is high. Thus, write assist transistor (WT) conducts. The data stored at nodes L and H determines which transistor (MP3 or MP4) isON. If node L (H) is storing logic '0' ('1'), transistor MP3 (MP4) isON. Thus, there exists a conductive path for RBLB (RBL) to discharge, the discharge path being MP3 (MP4) and RT.

As one of the bitlines discharges, voltage difference sets up between the two bitlines. A sense amplifier circuitry (not shown here) is used which senses the stored data, by sensing as soon as the voltage difference becomes 50mV [12].

While during read operation of single-ended SRAM cell [7] read word line (RWL) is turned high and read bitline RBL discharges if the data at node H is logic '1'. An inverter is connected to the read bitline (RBL). For single ended read operation the sense margin is 50% of the supply voltage, so that voltage at RBL decreases beyond switching threshold of the inverter [11]. In this paper the RBL is decreased up to 75% of the supply voltage to avoid misread. The read delay of the proposed DERD6T is estimated and compared with STD6T and SERD8T and reported in Table I. The same is plotted graphically in Fig. 5

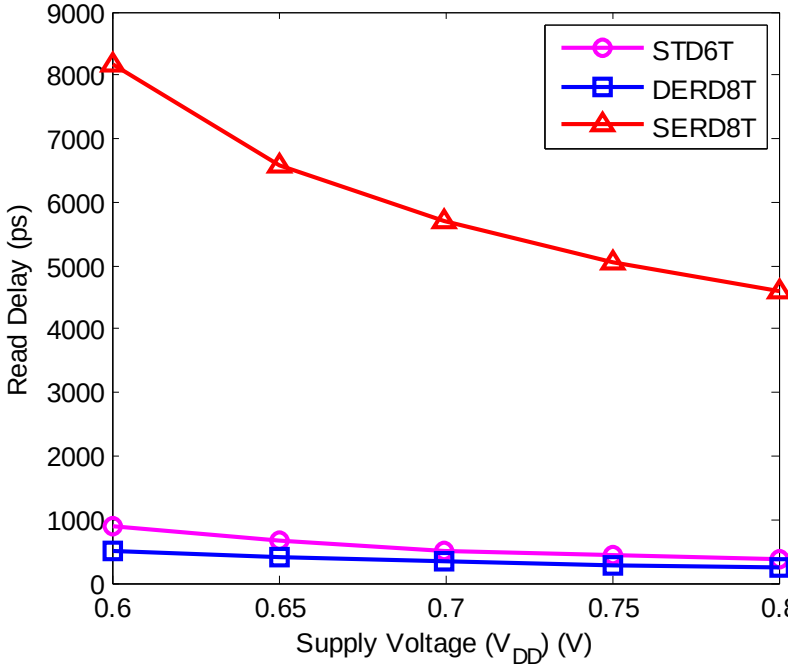

Fig. 5. Read Delay Vs Supply Voltage

TABLE I. READ DELAY OR READ ACCESS TIME

Supply Voltage (V)	Read Delay (ps)		
	STD6T	DERD8T	SERD8T
0.60	881	505	8170
0.65	653	391	6580
0.70	519	329	5700
0.75	431	286	5060
0.80	369	255	4610

. It can be seen that the read delay for the proposed DERD8T is shorter than the STD6T and SERD8T. A DTMOS (Dynamic threshold MOS) technique is employed in the read transistor (RT). Therefore, V_t of the transistor decreases as the body is connected to RL, which is made high during read operation. Hence, the RBLB/RBL dischargesat a faster rate.

B. Write Delay Analysis

During Write mode WL (word line) is made high, RBL and WLB (complementary word line) are turned low. The bitlines BL and BLB are loaded with data to be written. As WLB is low, WT does not conduct and weakens the feedback.

Write delay is measured as the difference between the time when WL reaches 50% of VDD and the time when node L, storing '0' attains 90% of the supply voltage (or H, storing '1' reaches to 10% of its initial voltage). The write of STD6T and SERD8T are same, as SERD8T cell is basically a standard 6T cell except the extra path for read operation and that has no influence on write operation. Therefore, write delay of STD6T and DERD8T are estimated and compared in a graphical form (Fig. 6). From the figure it can be seen that the proposed cell achieves shorter write delay due to the weakening of feedback.

C. Read Stability Estimation

Read static noise margin (RSNM) is the parameter used to estimate the cell's stability. The RSNM is defined as the minimum voltage which may flip the cell content [12], [17] during read operation. RSNM estimation is done by simulating the cell in read mode i.e. pulling WL to ground and turning RL to supply voltage.RSNM is estimated from the butterfly curves which is the VTCs (voltage transfer curves) during read operation as shown in Fig. 7.

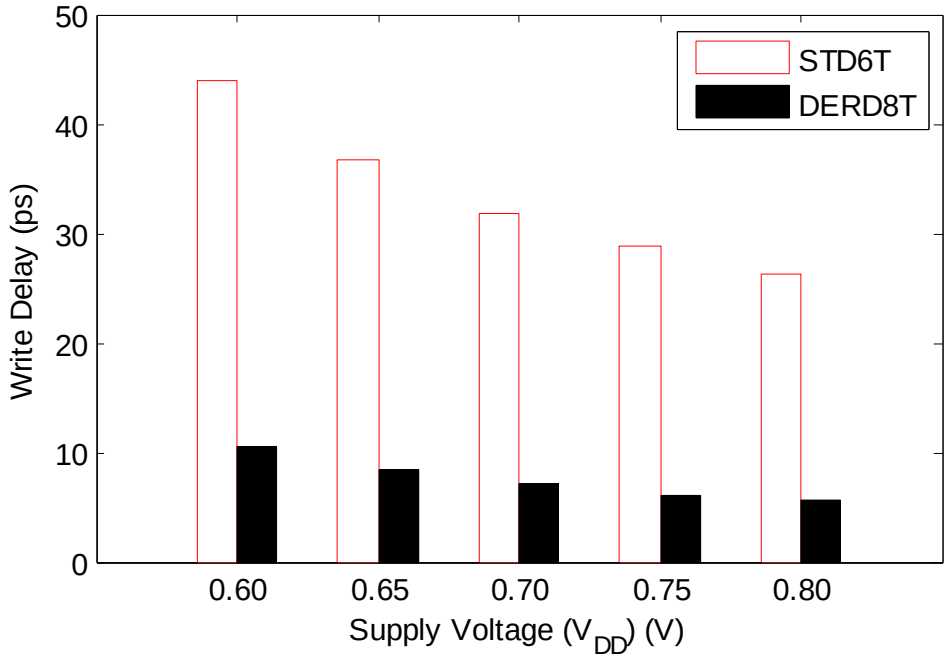

Fig. 6. Write Delay Vs Supply Voltage

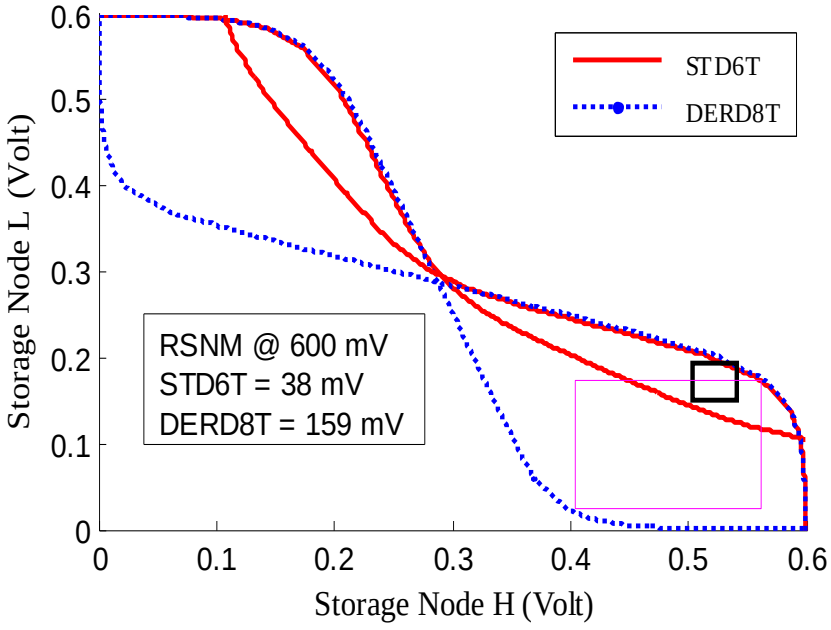

Fig. 7. Static VTC during READ operation

The side length of the largest square that can be fitted into the smaller lobe of the butterfly curve gives the correct measure of RSNM. From Fig. 7 it can be observed that RSNM of STD6T is 38 mV whereas the proposed cell has an RSNM of 159 mV @ 600 mV supply voltage. Therefore, the proposed DERD8T cell shows 4.18× improvements in read stability. The RSNM of STD6T is very low due to formation of voltage divider between access transistor and pull-down transistor. The voltage divider formed increases the voltage at node storing '0' which may result in flipping of thecell content.To avoid this, storage nodes must be read-decoupled. This fact is utilized in the proposed cell and in SERD8T cell. Different port is used for reading,

which decouples the storage node during read operation. Hence, RSNM of both the cells (DERD8T and SERD8T) are same and equal to hold SNM of STD6T. Thus, RSNM and hence read stability is improved.

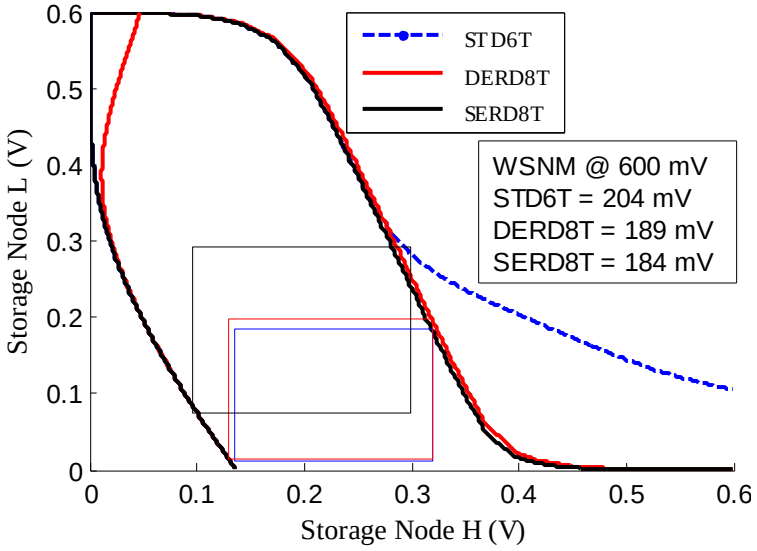

Fig. 8. Static VTC during read and write operation

D. Write Ability Estimation

WSNM (Write static noise margin) is the ability to flip the content of stage nodes. WSNM is calculated using read VTC and write VTC. The side length of the smallest square fitted in the lower half of the curve obtained from the combination of read VTC and write VTC (Fig. 8) gives the measure of WSNM [17]. From the figure it is noticed that DERD8T shows 1.07× lower WSNM compared to STD6T while it offers 2.71% improvement in WSNM compared to SERD8T cell.

IV. CONCLUSION

A simple double-ended read-decoupled 8T (DERD8T) SRAM cell is suggested in this paper. The proposed cell offers a considerable amount of improvement in read stability as compared to STD6T SRAM cell, as the storage nodes are read-decoupled. It also shows improvement in read delay. Furthermore, it offers shorter write delay compared to standard 6T cell. Therefore, the proposed cell is an attractive choice when stability of the cell and speed of memory are major requirement.

REFERENCES

[1] Semiconductor Industry Association (SIA), International Technology Roadmap for Semiconductors 2011 Edition. [Online]. Available: http://www.itrs.net/Links/2011ITRS/Home2011.htm.

[2] A. Bhavnagarwala, X. Tang, and J. Meindl, “The impact of intrinsic device fluctuations on CMOS SRAM cell stability”, IEEE J. Solid-State Circuits, vol. 36, no. 4, pp. 658-665, Apr 2001.

[3] A. Islam and M. Hasan, “Process Variation and Radiation-Immune Single Ended 6T SRAM Cell”, ACEEE Int. J. on Signal & Image Processing, Vol. 01, No. 03, Dec. 2010.

[4] A. Islam and M. Hasan, “SINGLE-ENDED 6T SRAM CELL TO IMPROVE DYNAMIC POWER DISSIPATION BY DECREASING ACTIVITYFACTOR”, The Mediterranean Journal of Electronics and Communications, Vol. 7, No. 1, pp. 172-181, 2011.

[5] R.E. Aly and M.A. Bayoumi, "Low-Power Cache Design Using 7T SRAM Cell," IEEE Trans. Circuits and Systems II: Express Briefs, vol.54, no.4, pp.318-322, Apr. 2007.

[6] A. Islam and M. Hasan, “A technique to mitigate impact of process, voltage and temperature variations on design metrics of SRAM Cell,” Microelectronics Reliability, vol. 52, no. 2, pp. 405-411, Feb. 2012.

[7] Chang, L.; Montoye, R.K.; Nakamura, Y.; Batson, K.A.; Eickemeyer, R.J.; Dennard, R.H.; Haensch, W.; Jamsek, D., An 8T-SRAM for Variability Tolerance and Low-Voltage Operation in High-Performance Caches," Solid-State Circuits, IEEE Journal of , vol.43, no.4, pp.956,963, April 2008

[8] N. Verma and A. Chandrakasan, "A 256 kb 65 nm 8T sub-Vt SRAM employing sense-amplifier redundancy," *IEEE J. Solid-State Circuits*, vol. 43, no. 1, pp. 141–149, Jan. 2008.

[9] B. H. Calhoun and A. Chandrakasan, "A 256 kb sub-threshold SRAM in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 42, no. 3, pp. 680–688, Mar. 2007.

[10] T. Kim, J. Liu, J. Keane, and C. H. Kim, "A high-density subthreshold SRAM with data-independent bitline leakage and virtual ground replica scheme," *IEEE J. Solid-State Circuits*, vol. 43, no. 2, pp.518–529, Feb. 2008.

[11] Ik Joon Chang; Jae-Joon Kim; Sang Phill Park; Roy, K., "A 32 kb 10T Sub-Threshold SRAM Array With Bit-Interleaving and Differential Read Scheme in 90 nm CMOS," Solid-State Circuits, IEEE Journal of , vol.44, no.2, pp.650,658, Feb. 2009

[12] A. Islam and Mohd. Hasan, "Leakage characterization of 10T SRAM cell," *IEEE Trans. Electron Devices*, vol. 59, no. 3, pp. 631 – 638, Mar. 2012.

[13] A. Islamand Mohd. Hasan, "Variability Aware Low Leakage Reliable SRAM Cell Design Technique," *Microelectronics reliability*, vol. 52, no. 6, pp. 1247 – 1252, Jun. 2012.

[14] D. Roy, A.K.singh, A.Islam, "Bitline and Storage Node Decoupled 13T SRAM cell in 22-nm Technology Node", Wulfenia, vol. 20, no. 3, pp. 40–55, Mar. 2013.

[15] Nanoscale Integration and Modeling (NIMO) Group, Arizona State University (ASU). [Online]. Available: http://ptm.asu.edu/.

[16] M. Barlow,et al., "A PFET-access radiation-hardened SRAM for extreme environments", *51st Midwest Symposium on Circuits and System-MWSCAS* 2008, pp.418-421, Aug.2008.

[17] S. Pal, A. Bhattacharya and A. Islam, "Comparative Study of CMOS- and FinFET-based 10T SRAM Cell in Subthreshold regime," *IEEE* Int. *Conf. on Advanced Communication Control and Computing Technologies (ICACCCT)*, pp. 507-511, May 2014.