

# A 4.596 GHz, High Slew Rate, Ultra low Power Cascode Operational Amplifier in 45nm CMOS for Wireless Communication

Ramkrishna Kundu<sup>1</sup>, Abhishek Pandey<sup>2</sup>, Dipayan Ghosh<sup>3</sup>, Jyoti Singh<sup>4</sup>, Vijay Nath<sup>5</sup> (Member IEEE)

VLSI Design Group, Department of ECE, B.I.T. Mesra, Ranchi-835215(JH), India

<sup>1</sup>ramkrishnakunduece@gmail.com <sup>2</sup>pandeyabhishekec123@gmail.com <sup>3</sup>dipayan2007@gmail.com  
<sup>4</sup>jyoti6242@gmail.com <sup>5</sup>vijaynath@bitmesra.ac.in

**Abstract**— In this paper we have proposed a low power, high slew rate, ultra wide band cascode operational amplifier for wireless communication systems. The proposed circuit is designed and simulated using Cadence analog and digital system design tools of gpdk45nm CMOS technology. This circuit simulated results are DC gain 22.44dB, unity gain bandwidth 4.596Ghz, 3dB bandwidth 422.2Mhz, slew rate 1678v/μs, phase margin 59 degree, rail to rail power supply of the proposed op-amp is ±1.5V and power consumption is 1.49mW. This circuit specification is fully meets the requirements of wireless communication systems.

**Keywords**—Op-amp (Operational Amplifier), CMOS (Complementary Metal Oxide Semiconductor Field Effect Transistor), Slew Rate, ISM (Industrial, Scientific and Medicine)

## I. INTRODUCTION

In 1965, G.E. Moore predicted that the no. of transistors in integrated circuits would be double in every 18 months .This statement has come true today. The method by which a large no. of transistor are assembled in a small silicon area is scaling. Scaling is the process by which the vertical and horizontal dimensions of MOSFETs are reduced. Because of the continuous transistors scaling into deep sub-micron dimensions it is possible to design integrated circuits for several multi-GHz wireless and wire line application. But due to this continuous scaling analog and mixed signal circuit design becomes challenging due to the short channel effects, increased channel length modulation, unwanted leakage etc.

Operational Amplifiers are the most generic building block of AMS system because of their wide range of application. In wireless application it is desirable that the op-amps should have considerable gain which is maintained to a wide bandwidth with moderate power consumption. Another criterion for the Op-Amps which will be used in wireless application is it should have high slew rate for avoiding distortion. We have found in literature [1]-[3] the op-amp whose gain is high but the unity gain band width is not suitable for wireless communication devices in ISM band. In [4]-[5] the gain and unity gain bandwidth is suitable for wireless communication in radio frequency but power dissipation and slew rate are not suitable for battery operated wireless communication devices.

This paper presents the cascode architecture of Op-amp that will deliver wide bandwidth, high slew rate and low power dissipation.

## II. METHODOLOGY

Active filters are the important building block of wireless communication. Op-Amp is one of the basic block of those filter .Most of the wireless communication devices are operated in radio frequency range. In Op-Amp feedback is used to make the transfer function independent to the gain of the Op-Amp. But if the frequency is

increased the gain of the Op-Amp decreases and the closed loop transfer function will not be independent of the gain of the Op-Amp. So the Op-Amp used for radio frequency filter should have ultra wide bandwidth. The conventional two stage Op-Amp can't deliver ultra wide bandwidth and their ICMR and PSRR is also decreases. The above mentioned problem can be resolved in cascode architecture .In cascode architecture the gain is increased by increasing the output resistance. The output resistance is inversely proportional to the bias current .So in cascode architecture, the gain can be improved by reducing the bias current and due to that the power consumption also reduces, cascoding can be done in the both stages of Op-Amp .Here cascoding is done on the second stage to avoid complexity of using level shifter while using cascoding in first stage. In the design of Op-amp gain and stability performance are opposite in nature. The proposed architecture will provide a tradeoff between the gain and stability. The schematic of Op-amp is shown in Fig.1.

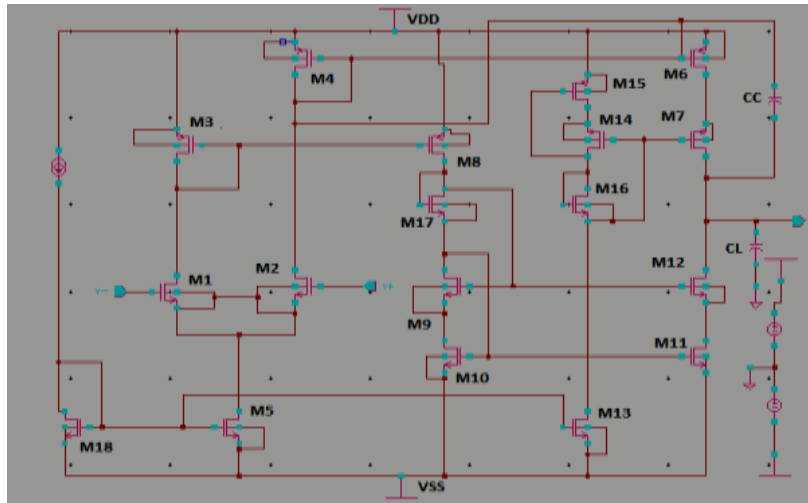


Fig.1. Schematic of proposed op-amp

We know that the unity gain bandwidth is given as-

$$GB = \frac{g_{mI}}{C_L}$$

$g_{mI}$  is the input transconductance and  $C_L$  is the capacitor that connected from output to the ground. So to obtain a very high unity gain bandwidth the input transconductance should be very high and the value of  $C_L$  should be small .The input transconductance is the transconductance of the transistor M1or M2.The transconductance is proportional to the square root of the channel width to channel length ratio. That's why the channel width of M1and M2 are made large and  $C_L$  made small. As slew rate is also inversely proportional to  $C_L$  .So slew rate also increases for small  $C_L$  .

In this Op-amp, To reduce gain of the first stage M3 and M4 are used as active load. Due to the reduction of the gain of first stage, the output pole of first stage has been increased as the lower resistance of M4 to AC ground. The output signal from the first stage is applied differentially to the cascode output stage. Most of the gain comes from second stage.

The gain from the first stage is [6]-[10].

$$A_{VI} = \frac{g_{m2}}{g_{m4}} = \frac{g_{m1}}{g_{m3}} \quad (1)$$

Here gm is the transconductance and suffix denotes the transistor number.

The gain from second stage is

$$A_{VII} = \left(\frac{g_{m6} + g_{m8}}{2}\right)R_{II} \quad (2)$$

$$R_{II} = \left(g_{m7}r_{ds7}r_{ds6}\right) \parallel \left(g_{m12}r_{ds12}r_{ds11}\right) \quad (3)$$

Here  $r_{ds}$  is the drain to source resistance.

So the overall gain

$$A_V = A_{V1}A_{VII} = \frac{g_{m2}}{g_{m4}} \left(\frac{g_{m6} + g_{m8}}{2}\right)R_{II} \quad (4)$$

As the dominant pole is now at the output, Op-amp is compensated by the shunt capacitance  $C_C$  at the output which can be classified as self compensation.

In this circuit  $M_{16}$  and  $M_{17}$  transistor are used as MOS resistor. As the fabrication of resistors are very tedious job, that is why resistors are replaced by MOSFET.

The channel length of the MOSFET in this circuit is 45nm. As the channel length is reduced this also contribute in the unity gain bandwidth enhancement. The unity gain frequency of a MOSFET is given by

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \quad (5)$$

Where  $g_m$  is transconductance of the MOSFET ,  $C_{gs}$  is gate to source capacitance,  $C_{gd}$  is gate to drain capacitance.

In saturation region

$$C_{gs} = \frac{2}{3} w l C_{ox} \quad (6)$$

$$C_{gd} = 0 \quad (7)$$

Where  $w$  is width of the channel ,  $l$  is length of the channel and  $C_{ox}$  is oxide capacitance per unit area. As length of the channel decreases  $C_{gs}$  and  $C_{gd}$  are also decreased and in effect  $f_T$  increases. So, we get the higher bandwidth.

### III. SIMULATION RESULT & DISCUSSION

The proposed Op-amp is shown in Fig.1 simulated using the Cadence analog and digital system design tools gpdk45nm technology. For simulation used rail to rail power supply is  $\pm 1.5V$ . The proposed Op-amp showed the unity gain bandwidth of 4.596 GHz, 3dB bandwidth of 422.2 MHz, DC gain of 22.44 dB, phase margin 59 degree slew rate of 1678V/ $\mu s$  and power consumption of 1.49mW.

The simulation results and used power supply are listed in Table 1. The gain and phase plot vs. frequency (AC response) of proposed Op-amp is shown in Fig.2.

TABLE. 1.  
Performance analysis of proposed op-amp

CMOS Technology	45nm
Power Supply	$\pm 1.5V$

DC Gain	22.44dB
Unity gain bandwidth	4.596GHz
3dB bandwidth	422.2MHz
Phase margin	59 Degree
ICMR	-1.487V to 200mV
CMRR	33.15dB
PSRR(Positive)	27.32dB
PSRR(Negative)	28.25dB
Offset Voltage	31.516mV
Slew rate	1678 V/ $\mu$ s
Settling Time	16.947nS
Power consumption	1.49mW
Core area	13.7 $\times$ 13.7 $\mu$ m <sup>2</sup>

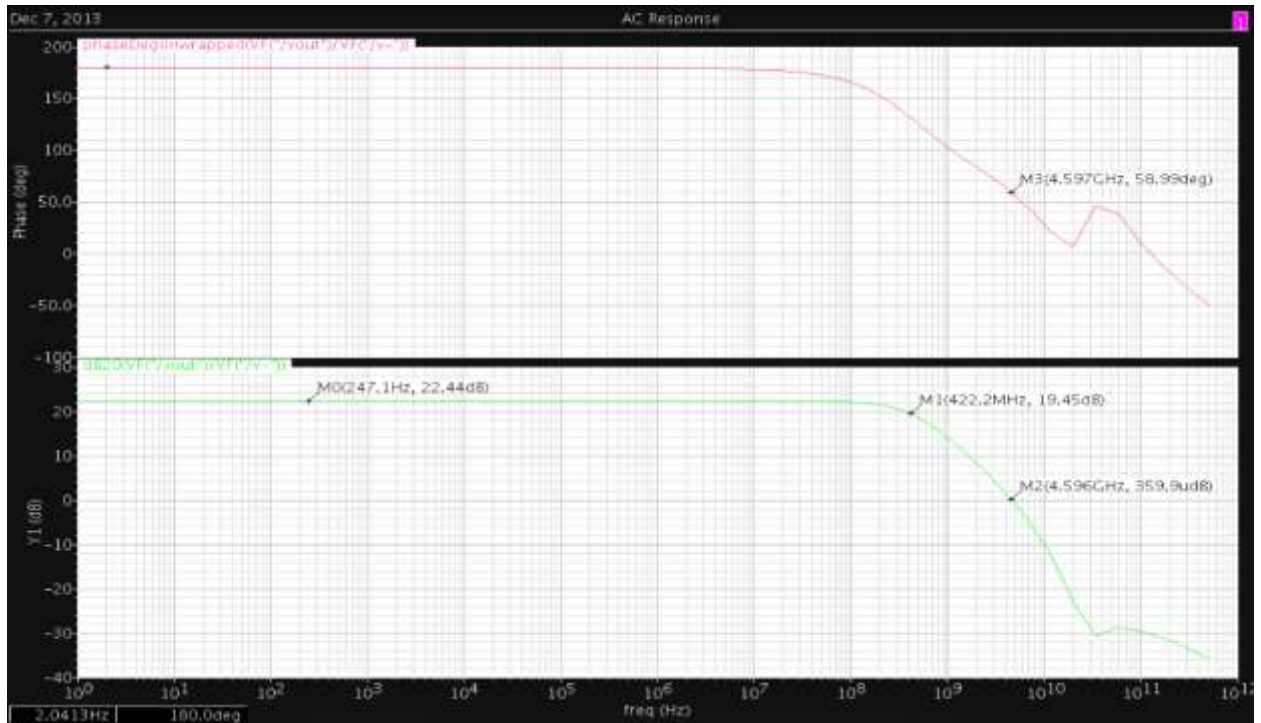


Fig. 2. Gain and phase plots vs. frequency (AC Response) of proposed Op-amp

The Lay out of the OpAmp is shown in the Fig.3

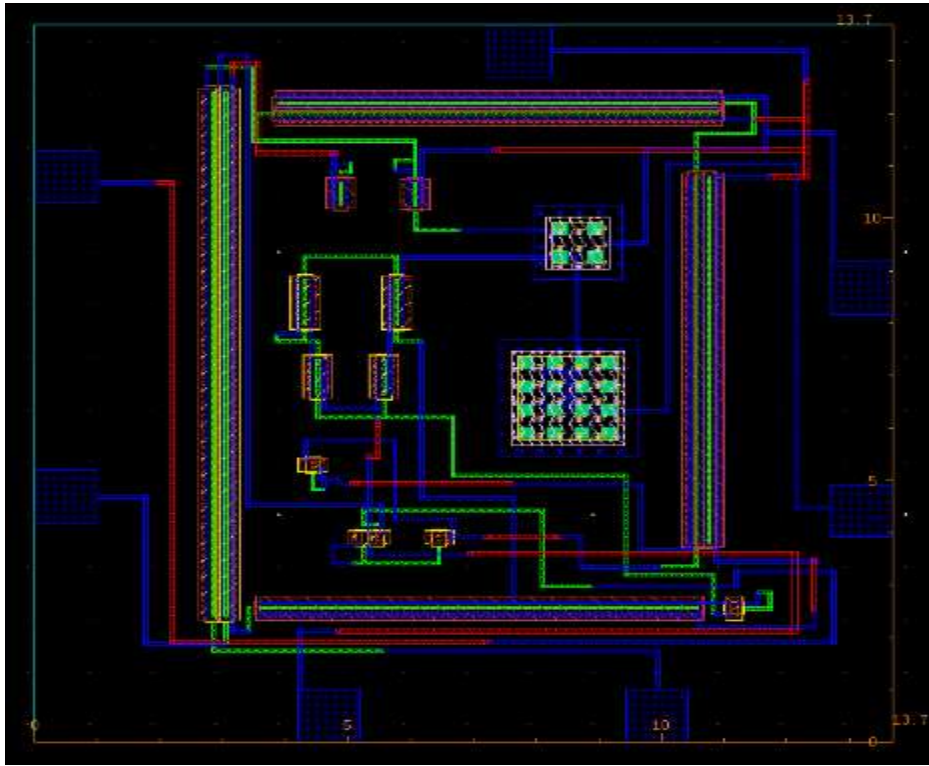


Fig.3 Lay out of the proposed of the Op Amp

Proposed Op-amp circuit result with existing Op-amp circuit published in recent year shown in TABLE-2

TABLE -2  
Cross Platform Comparative Performance

Parameters	This Work	[1]	[2]	[3]	[4]	[5]
Technology	45nm	180nm		65nm	180nm	40nm Digital CMOS
Supply Voltage(Volt)	1.5	1	1.8	-	1.8	1.1
Gain(dB)	22.44	73	60.5	58	65	49
Unity Gain Bandwidth (Hz)	4.55G	7.6M	538.3M	1G	2.3G	3.2G
Phase Margin(Degree)	59		59.64	62	58	-
Slew Rate	1678V/ $\mu$ s	-	-	-	>450V/ $\mu$ s	-

Power Dissipation	1.49mW	–	2.13mW	-	25mW	18.7mW
-------------------	--------	---	--------	---	------	--------

### CONCLUSION

In this paper low power CMOS Op-amp is proposed, it is simulated in cadence analog and digital 45nm technology. The designed schematic of Op-amp is useful in designing of filters for wireless application. For simulation rail to rail power supply is  $\pm 1.5V$ . The proposed Op-amp showed the unity gain bandwidth of 4.596GHz, 3dB bandwidth of 422.2 MHz, gain of 22.44dB, phase margin 59 degree, slew rate of 1678V/ $\mu s$  and power consumption of 1.49mW.

### ACKNOWLEDGMENT

We are thankful to Department of Science and Technology, New Delhi and Defense Research Development Laboratory Hyderabad India for funding this project. We are also thankful to our Vice-Chancellor, Dr. P.K. Barahai and our Head of Department, Dr. S.K.Ghorai for his constant inspiration and encouragement.

### REFERENCES

- [1] C.Guo, S. Zhu, J. Hu, J. J. Zou, H. Sun, X. Lv, "A Low Voltage CMOS rail to rail operational amplifier based on flipped differential pairs," IEEE Microwave, Antenna, Propagation and EMC Technologies for Wireless Communications (MAPE) 2011 IEEE 4<sup>th</sup> International Symposium on Digital Object Identifier, pp. 217–220, 2011.
- [2] T.K.Bhattacharyya, M.K.Hati (2012). "A Power Efficient and constant-gm 1.8 V CMOS Operational Transconductance Amplifier With Rail to Rail input and output ranges for charge pump in Phase locked loop," IEEE Circuit and Systems International conference on Digital Object Identifier, vol. 134, pp. 38–43, 2012.
- [3] H. Vhrmann, F. Schologl, V.Schweiger, H. Zimmermann "A 1 GHz-GBW Operational amplifier for DVB-H Receivers in 65nm CMOS," IEEE Design and Diagnostic of electronic circuits and systems, 2009.DDECS'09.12th International Symposium on Digital Object Identifier, pp. 182-185, 2009.
- [4] D. Gangopadhyay, T.K. Bhattacharyya, "A 2.3 GHz gm- boosted High Swing Class AB Ultra Wide bandwidth operational amplifier in 0.18 $\mu m$  CMOS," IEEE 53<sup>rd</sup> International Midwest Symposium on Circuit and systems (MWSCAS), pp. 713-716, August 2010.
- [5] Hong Chen, et.al., " Ultra high bandwidth fully Differential three stage operational amplifier in 40nm Digital CMOS, " Design and Diagnostics of electronic systems (DDECS), 2013 IEEE 16<sup>th</sup> International Symposium on Digital object identifier, pp. 76-81, 2013.
- [6] Razavi B., Design of CMOS Analog Integrated Circuits, McGraw Hill, California, 1998.
- [7] P.E.Allen, D.R. Holberg, CMOS Circuit Design, Oxford Indian Edition, 2009.
- [8] Gray, P. and Meyer, R., Analysis and Design of Analog Integrated Circuits, John Wiley & sons.
- [9] V. Nath, L.K. Singh, K.S. Yadav, " Design and Development of CMOS bandgap Voltage Reference Circuit in VLSI," International Journal of Systemic, Cybernetics and Informatics, vol-2, pp. 71-75. April 2007.
- [10] V.Nath, K.S. Yadav, L.K. Singh, " Modeling, Simulation and layout Design of CMOS signal conditioning circuit with M/NEMS Sensors in VLSI," Lucknow Nation Journal of Science, Vol.8, No.1, (2011), pp.59-69, available online: [www.indianjournals.com](http://www.indianjournals.com)