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# Low Power Low Voltage High Speed Circuit Design Using Strained Silicon

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***Abstract*- A technique to design a low power low voltage high speed circuit is proposed in this paper. Supply voltage of 3.3v is widely used at present for MOSFET devices. But power dissipation depends not only on the supply voltage bot also on different factors. Every designer has the target to reduce the power dissipation without compromising the speed of the circuit. If a MOSFET consumes less power and less voltage and provide high speed it can be used in large circuits. This paper will show how the power dissipation can be reduced by using strained silicon MOSFET.**

***Index Terms*- MOSFET, Gate Length, Threshold Voltage, Propagation Delay, Rise and Fall Time.**

## I. INTRODUCTION

This paper deals with various characteristics of MOSFET So the first question comes what is a MOSFET. It is a three terminal device. The basic principle involved is the voltage between two terminals of control the current flowing in the third terminal. Fig 1 shows the device structure of a MOSFET. The field effect transistor is fabricated on p-type substrate, which is a single crystal silicon wafer that provides physical support. Silicon di oxide (SiO2) is used on the surface of the substrate to cover the area between the source and drain regions. Metal is deposited on the top of the oxide to form the gate electrode of the device. That's why it is called" Metal Oxide Semiconductor Field Effect Transistor". Gate length of a MOSFET meaus the distance between the Source and Drain terminal. By reducing this length we can reduce the power dissipation. In this it will is shown that if we replace bulk silicon by strained silicon it will reduce the power dissipation without compromising the speed of the circuit.

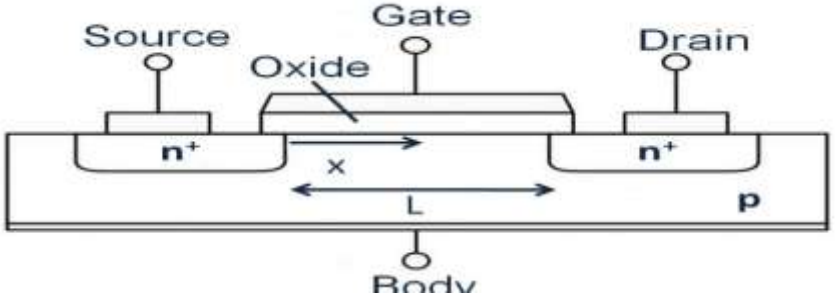



Figure: 1

## II. IDENTIFY, RESEARCH AND COLLECT IDEA

Some terminologies related to MOSFET as well this paper are Threshold voltage, Propagation Delay, Rise time, Fall time. Now let us be familiar with each terminology.

*Threshold voltage:* Threshold voltage is defined as the minimum voltage that required to make the transistor ON. Transistor maybe either NMOS or PMOS. For NMOS the threshold voltage is positive and for PMOS the threshold voltage is negative.

The threshold voltage ( Vth) of a field effect transistor (FET) is the value of the gate-source voltage(Vgs) when the conducting channel just begins to connect the source and drain contacts of the transistor, allowing significant current to flow. If Vgs is less than Vth then there will be no current flow.

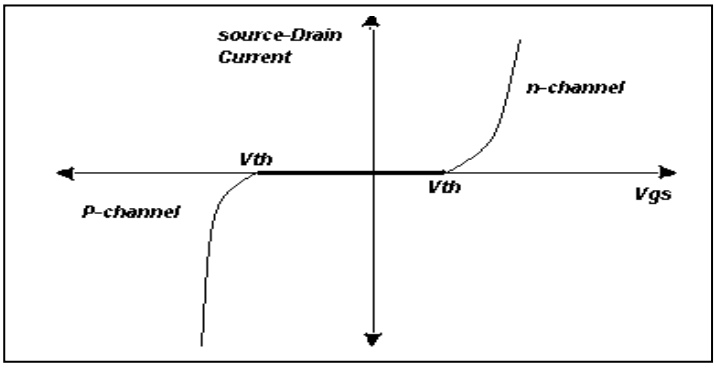



Figure: 2

*Propagation delay:* When gate inputs change, output doesn't change instantaneously. This delay is known as Propagation delay.

Time it takes for a change at the input of a device to produce a change at the output of the same. Two types of propagation delays are there when the output changes from Low to High and High to Low.

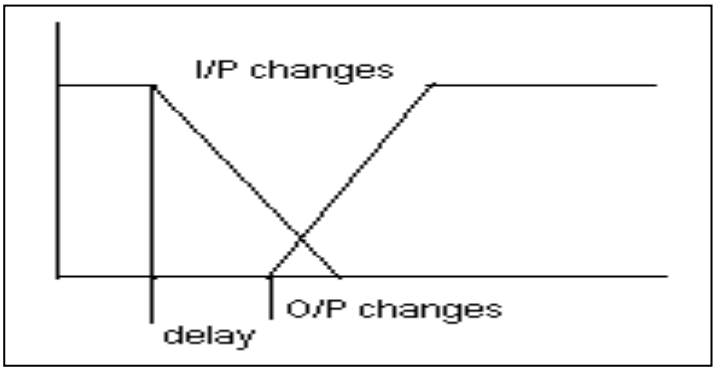



Figure: 3

*Rise Time:* Rise time is the difference between the time when the signal crosses a low threshold to the time when the signal crosses the high threshold. It can be absolute or percent.

*Fall Time:* Rise time is the difference between the time when the signal crosses a high threshold to the time when the signal crosses the low threshold. It can be absolute or percent.

Figure 4 shows the Rise and Fall time

The Rise time and the fall time should be small compared to the clock period. Very large Rise time and fall time have the risk of the cycles going undetected. Large Rise and Fall time mean that the signal will be hovering around mid level for too long making the system highly susceptible to noise and multiple triggering if there is not enough hysteresis

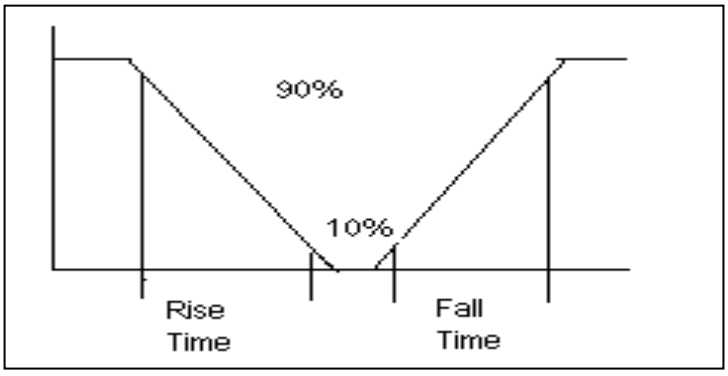



Figure:4

*Literature review:*
Power Dissipation has three components.-

*Static power:* The semiconductor consumes some power due to the leakage in Transistors. The leakage current also generates heat that leads to degraded performance. The term leakage current refers to the unintended power loss from a capacitor. When a capacitor is powered off a small amount of current passes through which causes the power dissipation.
Pstat=Vdd*Ileak ---------- (1)

*Dynamic capacitive power:*
Power Dissipation (Pdynamic)= Vdd2*CL*Fop ----------(2)
Equation 2 is the equation of power dissipation where Vdd is the Supply Voltage, CL is the Load capacitance, Fop is the Operating Frequency. From the equation it is clear that if we can reduce the three component of the equation we can reduce the power.

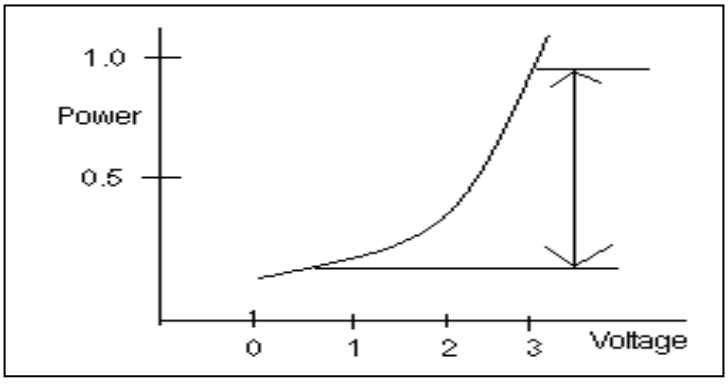



Figure 5

Decreasing Capacitance is difficult as it need to scale down the device and wiring.
some time higher frequency is needed for Better throughput performance. Introducing Parallel processing lower frequency can be applied but it increases Hardware overhead and requires extrusive change at an architecture or algorithm design. If we can reduce the supply voltage from 3.3 v to 1v power dissipation will be reduced 10 times as it is shown in the figure 5 . But if we reduce supply voltage we have to compromise the speed because of the drastic increase in Gate delay time. One way to overcome this problem is to reduce the Threshold voltage of MOSFET.

*Dynamic short-circuit power:* This is the power cousumption due to the Short circuit current or the direct current path between the supply voltage nd the ground. It happeus during the finite slope of the input signal as shown in fig. 6.
Psc=Tsc*Vdd*Imax ----------(3)

Tsc is the duration of the slope of the input signal. This component is directly depended on the Rise time and Fall time.

Tsc=(Trise+Tfall)\2----------(4)

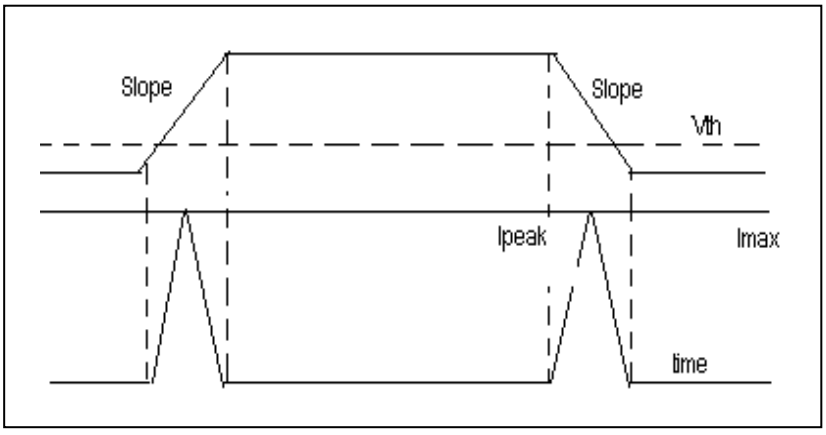



Figure 6

From this equation we can say that fast Rise time , Fall time on input signal meaus lower short circuit power dissipation.

Total power dissipation ($P_{tot}$)= $P_{stat}$+$P_{dynamic}$+$P_{sc}$----------(5)

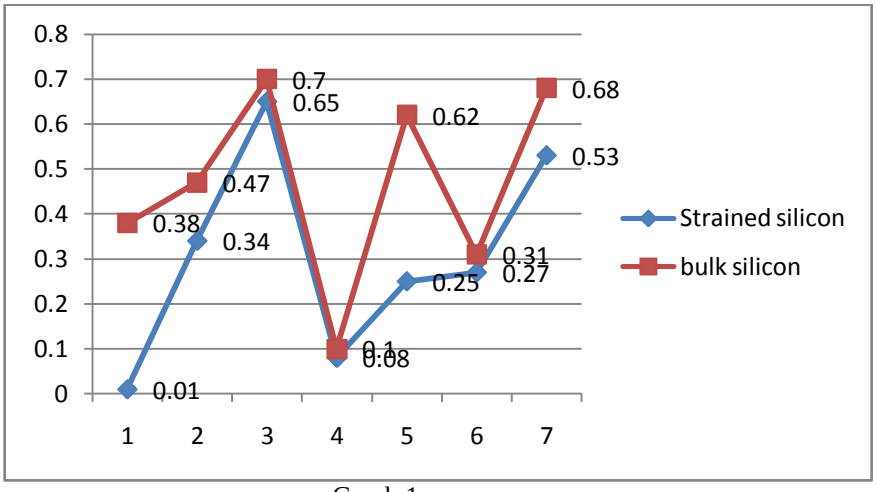
Reducing Static power consumption we can reduce the total power consumption.

*Introduction to strained silicon:* Strained silicon is a layers of silicon in which the silicon atoms are streached beyond their normal inter atomic distance. This can be accomplished by putting the layer of silicon over a substrate of silicon germanium (SiGe). As the atoms of silicon layer align with the atoms of the underlying silicon germanium layer, the links between the silicon atoms become stretched-thereby leading to strained silicon.

*Advantages of strained silicon over bulk silicon:* Moving these silicon atoms farther apart reduces the atomic forces that interfere with the movement of electrons through the transistors and thus better mobility and better chip performance can be achieved. These electrons can move 70% faster allowing strained silicon transistors to switch 5% faster.

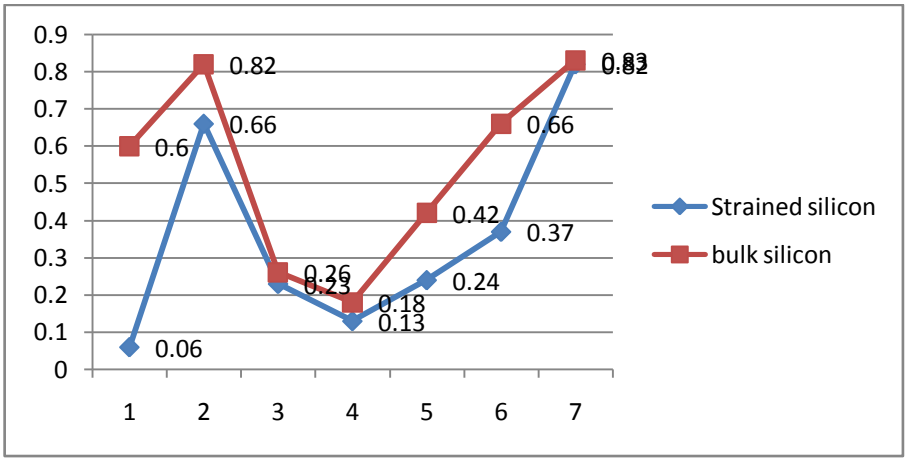
## III. RESULTS AND DISCUSSIONS

Our target is to reduce the power dissipation and increase the speed. As I have already shown that reducing the Rise time and Fall time we can reduce the power dissipation. To get better speed we need to reduce the propagation delay. Reducing the gate length of the MOSFET we can achieve both the things. Now it is the time to show the result. To prove this I have taken the help of PSPICE as simulation software. Using this I have designed all the basic gates like Inverter, AND, OR NAND, NOR, Half Adder and Full adder. I have calculated the Rise time, fall time and the Propagation delay of all the circuits made of silicon and strained silicon both.



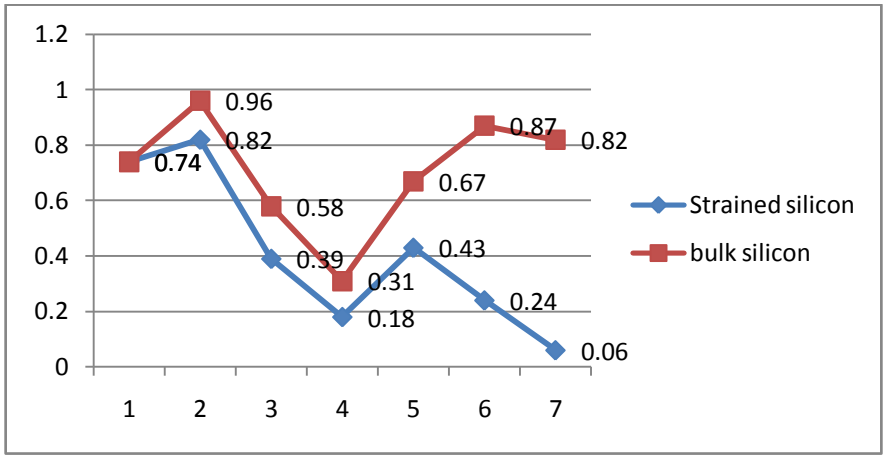

Graph 1

Graph 1 shows that propagation delay from Low to High for all the gates where we can see that the delay is always less for strained silicon.



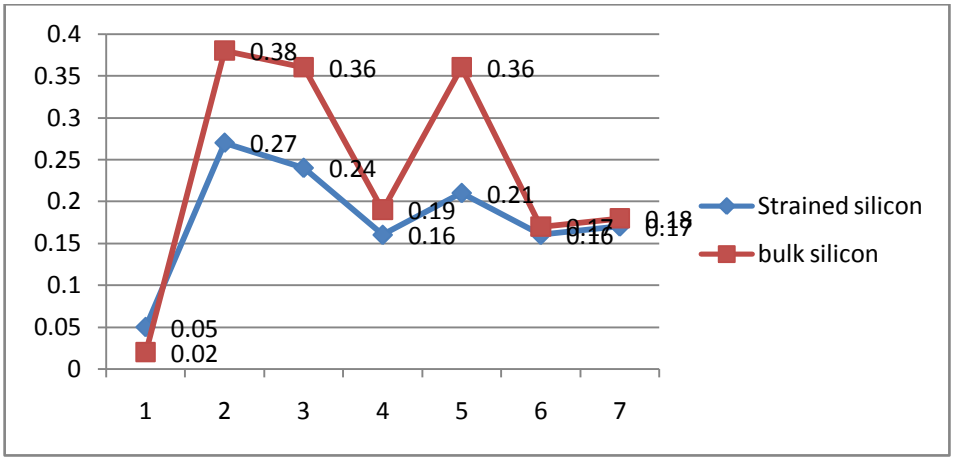

Graph 2

Graph 2 shows that propagation delay from High to Low for all the gates where we can see that the delay is always less for strained silicon.




Graph 3

Graph 3 shows the Rise time for all the gates where we can see that the delay is always less for strained silicon.




Graph 4

Graph 4 shows the Fall time for all the gates where we can see that the delay is always less for strained silicon.

## IV. CONCLUSION

From the result it is proved that if the substrate is replaced by strained silicon then the delay is reduced. The performance speed also depends on the delay. That means to improve the performance we need to replace silicon by strained silicon. The short circuit power consumption is a component of total power dissipation. The short circuit power dissipation can be reduced by reducing the Rise time and Fall time of the input signal. From the result it is also proved that Rise time and Fall time can be reduced by introducing strained silicon. That means total power dissipation is also less in case of strained silicon MOSFET. Finally we can conclude that to get a low power high speed circuit we have to replace the silicon substrate of the MOSFET by strained silicon.

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